Michael J. Wirthlin

Associate Professor
Department of Electrical and Computer Engineering
Brigham Young University
459 Clyde Building
Provo, UT 84602

TEL: (801) 422-7601
FAX: (801) 422-0201
Email: wirthlin@ee.byu.edu
http://www.ee.byu.edu/faculty/wirthlin

Education:

Ph.D. Brigham Young University, Provo, UT - Electrical and Computer Engineering
Dissertation: Improving Functional Density Through Run-Time Circuit Reconfiguration
August 1997

B.S. Brigham Young University, Provo, UT - Electrical and Computer Engineering
August 1992, Suma Cum Laude with University Honors
Honors Thesis: A Quantitative Study of RISC Pipelining Techniques Using Custom Software Simulation Tools

Areas of Specialization:

FPGA Reliability
Digital Circuit Design
FPGA Circuit Design
High-Level Synthesis
Reconfigurable Computing Architectures
Application-Specific Computing Architectures
Reliable Computing

Professional Experience:

Associate Professor (1999 – present)
Dept. of Electrical and Computer Engineering, Brigham Young University, Provo, UT
- Graduate and undergraduate teaching in Computer Engineering and Digital Design
- Research in configurable computing architectures, application-specific computing, application-specific synthesis approaches, FPGA reliability, application-specific signal processing architectures, and configurable system on chip

Staff Engineer (1997-1998)
National Semiconductor, Architecture Laboratory, Santa Clara, CA
- Investigate and develop system design methodologies for single-chip systems
- Create system performance modeling for embedded system on chip architectures

Design Engineer (1992-1994)
National Technology Incorporated, Salt Lake City, UT
- FPGA design of digital sound products
- Configurable computing architecture development

Controls Engineer, Co-Op (1990-1991)
Saturn Corporation, Lost Foam and Vehicle Systems Operations, Spring Hill, TN
- PLC programmer for automobile manufacturing facility

Professional Activities

Senior Member of the IEEE, member of IEEE Computer Society
Member of the Association for Computing Machinery (ACM), Tau Beta Pi
Technical Program Co-Chair for the International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2010)

Technical program committee and publicity chair for International Conference on Field Programmable Logic and Applications (FPL 2008-2009)
Reviewer for *IEEE Transactions on VLSI Systems*, *Kluwer Journal of VLSI Signal Processing*, *IEEE Computer Magazine*, ACM Design Automation Conference, IEEE Symposium on Field-Programmable Custom Computing Machines, IEEE Transactions on Computers, and the International Symposium on Signal Processing and its Applications (ISSPA).
Review panelist for the National Science Foundation
Technical program committee for ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, International conference on Engineering of Reconfigurable Systems and Algorithms, and International Conference on Military and Aerospace Programmable Logic Devices (MAPLD).
Special session organizer (Reconfigurable System on Chip Architectures), International conference on Engineering of Reconfigurable Systems and Algorithms (2004)
Department graduate coordinator (2006 – 2009)
University Sailing Club Advisor (2004 – 2009)
Member of ACM/SIGDA DAC PhD forum organizing committee (2002-2004)

Awards:

Outstanding Faculty Award, Dept. of Electrical and Computer Engineering, 2007.

Courses Taught:

ECEN 220/224s: Introductory Digital Design and State Machines
ECEN 320: Advanced Digital Design
ECEN 427: Embedded Systems
ECEN 490: Senior Project (Computer System Design Project, FPGA Software Radio Project)
ECEN 522r: Computer System Reliability
ECEN 528: Advanced Computer Architecture
ECEN 625: Synthesis and Optimization of Digital Circuits
Reliability class, graduate seminar
ECEN 682r: Graduate Seminar

Courses Developed:

Computer System Reliability: Developed a new three credit hour graduate course that includes reliability modeling concepts and fault tolerant computer system design techniques.

Advanced Digital Design Course: Developed a new five credit hour junior level digital design course to include relevant topics and more advanced material.

Advanced Digital Design Laboratory: Initiated the use of FPGAs in undergraduate teaching laboratories. Organized laboratory sequence for students to design and test a simple 16-bit processor.

Synthesis and Optimization of Digital Circuits: Introduced a new graduate course on digital circuit synthesis with an emphasis on scheduling and resource sharing.

Computer Systems Senior Project: Introduced a new senior project involving the specification, design, and testing of a complete computer system (hardware and software). Students taking this class participated in the IEEE Computer Society International Design Competition (CSIDC) and placed 3rd in the 2001 finals in Washington D.C.

Publications:

Journal Publications

1. A. Propst, K. Peters, M. A. Zikry, S. Schultz, W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, "Assessment of damage in composite laminates through dynamic, full-spectral interrogation of fiber Bragg grating sensors", *Smart Materials and Structures*, Vol 19, Structures and Materials, p. 1-11, Jan. 2010.

2. Patrick Ostler, Michael P. Caffrey, Derrick Gibelyou, Paul S. Graham, Keith S. Morgan, Brian H. Pratt, Heather M. Quinn, and Michael J. Wirthlin, "SRAM FPGA Reliability Analysis for Harsh Radiation Environments", *IEEE Transactions on Nuclear Science (NSREC)*, Vol. 56, No. 6, pp. 3519-3526, December 2009.

3. Heather Quinn, Paul Graham, Michael Wirthlin, Brian Pratt, Keith Morgan, Michael Caffrey, and Jim Krone, "A Test Methodology for Determining Space-Readiness of Xilinx SRAM-based FPGA Devices and Designs", *IEEE Transactions on Instrumentation and Measurement*, Vol. 58, No. 10, pp. 3380-3395, October 2009.

4. S. Schultz, W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, A. Propst, M. Zikry and K. Peters, "Full-spectrum interrogation of fiber Bragg grating sensors for dynamic measurements in composite laminates," *Smart Materials and Structures*, vol. 18, p. 115015, Sept. 2009.

5. Brian Pratt, Michael Caffrey, James F. Carroll, Paul Graham, Keith Morgan, and Michael Wirthlin, "Fine-Grain SEU Mitigation for FPGAs Using Partial TMR", *IEEE Transactions on Nuclear Science*, Vol. 55, No. 4, pp. 2274-2280, August 2008.

6. M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Pritchard, P. Palazzari, G. Kuzmanov, "OpenFPGA CoreLib Core Library Interoperability Effort", *Journal of Parallel computing*, Vol. 34, No. 4-5, pp. 231-244. 2008.

7. Brent E. Nelson, Brad L. Hutchings, and Michael J. Wirthlin, "Design, Debug, Deploy: The Creation of Configurable Computing Applications", *Journal of Signal Processing Systems*, Vol. 53, No. 1-2, pp. 187-196. 2008.

8. Keith Morgan, Daniel McMurtrey, Brian Pratt, and Michael Wirthlin, "A Comparison of TMR With Alternative Fault-Tolerant Design Techniques for FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 54, No. 6, Part 1, pp. 2065 - 2072, December 2007.

9. Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer, "FPGA Pipeline Synthesis Design Exploration Using Module Selection and Resource Sharing", *IEEE Transactions on Computer Aided Design*, Vol. 26, No. 2, pp. 254-265, February 2007.

10. Maya Gokhale, Paul Graham, Michael Wirthlin, D. Eric Johnson, and Nathaniel Rollins, "Dynamic Reconfiguration for Management of Radiation-Induced Faults in FPGAs", *International Journal of Embedded Systems*, Vol. 2, No. 1/2, pp. 28-38, 2006.

11. Keith Morgan, Michael Caffrey, Paul Graham, Eric Johnson, Brian Pratt, and Michael Wirthlin, "SEU-Induced Persistent Error Propagation in FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 52, No. 6, Part 1, pp. 2438 - 2445, December 2005.

12. D. Eric Johnson, Michael Caffrey, Paul Graham, Nathan Rollins, and Michael Wirthlin, "Accelerator Validation of an FPGA SEU Simulator", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 6, pp. 2147-2157, December 2003.

13. Paul Graham, Michael Caffrey, D. Eric Johnson, Nathan Rollins, and Michael Wirthlin, "SEU Mitigation for Half-Latches in Xilinx Virtex FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 6, pp. 2139-2146, December 2003.

14. Michael J. Wirthlin, "Constant Coefficient Multiplication Using Look-up Tables", *Journal of VLSI Signal Processing*, Vol. 36, pp. 7-15, 2004.

15. Edward A. Lee, Stephen Neuendorffer, and Michael J. Wirthlin, "Actor-Oriented Design of Embedded Hardware and Software Systems", Invited paper to the *Journal of Circuits, Systems, and Computer,* Vol. 12, No. 3, pp. 231-260, June 2003.

16. Michael J. Wirthlin and Brian McMurtrey, "Web-Based IP Evaluation and Distribution Using Applets", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems,* Vol. 22, No. 8, pp. 985-994, August 2003.

17. B. L. Hutchings, B. Nelson and M. J. Wirthlin, "Designing and Debugging Custom Computing Applications", *IEEE Design and Test of Computers*, Vol. 17, No. 1, pp. 20-28, January 2000.

18. M. J. Wirthlin and B.L. Hutchings, "Improving Functional Density Using Run-Time Circuit Reconfiguration", *IEEE Transactions on VLSI Systems*, vol. 6, no. 2, pp. 247-256, 1998.

Conference Publications, Full Paper Peer Review

19. Michael Caffrey, Kim Katko, Anthony Nelson, Joseph Palmer, Scott Robinson, Diane Roussel-Dupre, Anthony Salazar, Michael Wirthlin, William Howes, Daniel Richins, "The Cibola Flight Experiment", *23 Annual AIAA/USU Conference on Small Satellites*, August 2009.

20. Brian Pratt, Michael Caffrey, Paul Graham, Keith Morgan, and Michael Wirthlin, "Analysis of SEU-induced Errors in the Matched Filter of an FPGA-based Digital Communications Receiver", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 38-43, August 2009.

21. Jonathan Heiner, Benjamin Sellers, Michael Wirthlin and Jeff Kalb, "FPGA Partial Reconfiguration via Configuration Scrubbing", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 99-104, August 2009.

22. Benjamin Sellers, Jonathan Heiner, Michael Wirthlin, and Jeff Kalb, "Bitstream Compression Using Partial Reconfiguration", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 476-480, August 2009.

23. Adam Arnesen, Nathaniel Rollins, and Michael Wirthlin, "A Multi-Layered XML Schema and Design Tool for Reusing and Integrating FPGA IP", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 472-475, August 2009.

24. Michael Caffrey, Michael Wirthlin, William Howes, Daniel Richins, Diane Roussel-Dupre, Scott Robinson, Anthony Nelson, and Anthony Salazar, "On-Orbit Flight Results from the Reconfigurable Cibola Flight Experiment Satellite (CFESat)", *IEEE Symposium on Field Programmable Custom Computing Machines (FCCM 2009)*, pp. 3-10, April 2009.

25. Brian Pratt, Michael Caffrey, Derrick Gibelyou, Paul Graham, Keith Morgan, and Michael Wirthlin, "TMR with More Frequent Voting for Improved FPGA Reliability, " *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2008)*, pp. 153-158, July 2008.

26. Brent Nelson, Michael Wirthlin, Brad Hutchings, Peter Athanas, and Shawn Bohner, "Design Productivity for Configurable Computing", *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2008)*, pp. 57-66, June 2008.

27. Heather Quinn, Paul Graham, Keith Morgan, Jim Krone, Michael Caffrey, and Michael Wirthlin, "An Introduction to Radiation-Induced Failure Modes and Related Mitigation Methods for Xilinx SRAM FPGAs", *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2008)*, pp. 139-145, June 2008.

28. Jonathan Johnson, William Howes, Michael Wirthlin, Daniel McMurtrey, Michael Caffrey, Paul Graham and Keith Morgan, "Using Duplication with Compare for On-line Error Detection in FPGA-based Designs", IEEE Aerospace, Paper 1255.

29. Jonathan Heiner, Nathan Collins, Michael Wirthlin, "Fault Tolerant ICAP Controller for High-Reliable Internal Scrubbing", *IEEE Aerospace*, Paper 1256.

30. Brian Pratt, Michael Caffrey, James F. Carroll, Paul Graham, Keith Morgan, and Michael Wirthlin, "Fine-Grain SEU Mitigation for FPGAs Using Partial TMR", 9th European Conference on Radiation and Its Effects on Components and Systems (RADECS 2007), 2007.

31. Matthew French, Li Wang, and Michael Wirthlin, "Power Visualization, Analysis, and Optimization Tools for FPGAs", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 185-191. April 2006.

32. Brian Pratt, Michael Caffrey, Paul Graham, Keith Morgan, and Michael Wirthlin, "Improving FPGA Design Robustness with Partial TMR", *IEEE International Reliability Physics Symposium (IRPS)*, pp. 226-232, April 2006.

33. Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer, "Combining Module Selection and Resource Sharing for Efficient FPGA Pipeline Synthesis", *2006 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2006)*, pp. 179-188, February 2006.

34. Michael J. Wirthlin, "Senior-Level Embedded Systems Design Project Using FPGAs", Proceedings of the 2005 IEEE International Conference on Microelectronic Systems Education (MSE '05), pp. 91-92, June 2005.

35. Maya Gokhale, Paul Graham, Eric Johnson, Nathan Rollins, and Michael Wirthlin, "Dynamic Reconfiguration for Management of Radiation-Induced Faults in FPGAs", 11th Annual Reconfigurable Architectures Workshop (RAW 2004), Sante Fe, NM, 2004. pp. 145 - 152, ISBN 0-7695-2132-0.

36. Michael J. Wirthlin, "Computer Systems Design Competition at BYU", *2003 Frontiers in Education, IEEE Education Society*, pp. F1F-15 – F1F-21, November 2003.

37. Michael J. Wirthlin, Eric Johnson, Nathan Rollins, Michael Caffrey, and Paul Graham , "The Reliability of FPGA Circuit Designs in the Presence of Radiation Induced Configuration Upsets", *Proceedings of the 2003 IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 133-142. April 2003.

38. W. Landaker and M. J. Wirthlin, "Multitasking Hardware on the SLAAC1-V Reconfigurable Computing System", *12th International Conference on Field Programmable Logic and Applications (FPL-2002)*, pp. 806-815, August 2002.

39. M.J. Wirthlin and B. McMurtrey, "IP Delivery for FPGAs Using Applets and JHDL", *Proceedings of the 39th Design Automation Conference (DAC)*, pp. 2-7, June 2002.

40. E. Johnson, M. J. Wirthlin, and M. Caffrey, "Single-Event Upset Simulation on an FPGA", *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2002)*, pp. 68-73, June 2002.

41. M. J. Wirthlin and B. McMurtrey, "Efficient Constant Coefficient Multiplication Using Advanced FPGA Architectures", *Proceedings of the 11th International Workshop on Field-Programmable Logic and Applications (FPL)*, pp 555-564, August 2001.

42. M. J. Wirthlin, B. L. Hutchings and C. Worth, "Synthesizing Hardware from Java Byte Codes", *Proceedings of the 11th International Workshop on Field-Programmable Logic and Applications (FPL)*, pp 123-132, August 2001.

43. M. J. Wirthlin and N. Sundaramoorthy, “Measuring the Routing Costs of FPGA Circuit Components”. *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications*, Volume I, pp 129-134, June 2000.

44. M. J. Wirthlin, S. Morrison, P. Graham and B. Bray, “Improving Performance and Efficiency of an Adaptive Amplification Operation Using Configurable Hardware”, *Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines*, pp. 267-275, April 2000.

45. M. J. Wirthlin and B.L. Hutchings, “Improving Functional Density Through Run-Time Constant Propagation”, *1997 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 86-92, February 1997.

46. M.J. Wirthlin and B.L. Hutchings, “Sequencing Run-Time Reconfigured Hardware with Software”*, 1996 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 122-128, February 1996.

47. M.J. Wirthlin and B.L. Hutchings, “A Dynamic Instruction Set Computer”, *Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines*, pp. 99 - 107, April 1995.

48. M.J. Wirthlin and B.L. Hutchings, “DISC: The Dynamic Instruction Set Computer”*, Field Programmable Gate Arrays (FPGAs) for Fast Board Development and Reconfigurable Computing*, John Schewel, Editor, Proc. SPIE 2607, pp. 92-103 (1995).

49. B.L. Hutchings and M.J. Wirthlin, “Implementation Approaches for Reconfigurable Logic Applications”, *5th International Workshop on Field Programmable Logic and Applications*, pp 419-428, August 1995.

50. M.J. Wirthlin, K.L. Gilson, and B.L. Hutchings, “The Nano Processor: A Low Resource Reconfigurable Processor”, *Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines*, pages 23-30, April 1994.

Conference Publications, Abstract Review

51. W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, S. Schultz, A. Propst, K. Peters, M. Zikry, "High repetition-rate full-spectrum interrogation of FBG sensors for dynamic measurements in composite laminates," Proc. SPIE, vol. 7293, Mar. 2009.

52. Nathaniel Rollins, Adam Arnesen, and Michael Wirthlin, “An XML Schema for Representing Reusable IP Cores for Reconfigurable Computing”, *Proceedings of the 2008 National Aerospace and Electronics Conference (NAECON 2008)*, July 2008.

53. Wesley Kunzler, Zixu Zhu, Richard Selfridge, Stephen Schultz, Michael Wirthlin, “Integrating Fiber Bragg Grating Sensors with Sensor Networks”, *IEEE AUTOTESTCON*, September 2008.

54. Wesley Kunzler, Jason Newman, Daniel Wilding, Richard Selfridge, Stephen Schultz, Michael Wirthlin, and Andres Rodriguez, “Miniature MAV Telemetry Using a Portable Integrated FOS System”, *Proc. SPIE 6530 -- Sensor Systems and Networks: Phenomena, Technology, and Applications for NDE and Health Monitoring*, Paper 653005, 2007.

55. Michael J. Wirthlin and Welson Sun, "DSynth: A Pipeline Synthesis Environment for FPGAs", *IEEE Symposium on Field-Programmable Custom Computing Machines* (short paper), pp. 343-344. April 2006.

56. Matthew French, Paul Graham, Michael Wirthlin, and Li Wang, "Cross Functional Design Tools for Radiation Mitigation and Power Optimization of FPGA Circuits", Earth Science Technology Conference, NASA, Washington D.C., June 2006.

57. Brian Pratt, D. Eric Johnson, Michael J. Wirthlin, Michael Caffrey, Keith Morgan, and Paul Graham, “Improving FPGA Design Robustness with Partial TMR”, *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.

58. Matthew French, Paul Graham , Michael Wirthlin, Li Wang, Gregory Larchev, "Radiation Mitigation and Power Optimization Design Tools for Reconfigurable Hardware in Orbit", Earth Science Technology Conference, NASA, Washington D.C., June 2005.

59. Nathan Rollins, Michael J. Wirthlin, Michael Caffrey, and Paul S. Graham, "Evaluation of Power Costs in Applying TMR to FPGA Designs", 7th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), Washington D.C., 2004, Paper P136.

60. D. Eric Johnson, Keith S. Morgan, Michael J. Wirthlin, Michael Caffrey, and Paul S. Graham, "Persistent Errors in SRAM-based FPGAs", 7th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), Washington D.C., 2004, Paper P135.

61. M. French, P. Graham, and M. Wirthlin, "Design Tools for Reconfigurable Hardware in Orbit", NASA Earth Science Technology Conference 2004, Palo Alto, CA, June 22-24. ISBN 0-9721439-6-3.

62. Nathan Rollins, Michael Wirthlin, Paul Graham, and Michael Caffrey, "Evaluating TMR Techniques in the Presence of Single Event Upsets", *6th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, Paper P63 September 2003.

63. Michael J. Wirthlin, Nathan Rollins, Michael Caffrey, and Paul Graham, "Hardness by design techniques for field-programmable gate arrays", *Proceedings of the 11th Annual NASA Symposium on VLSI Design*, Coeur d'Alene, ID, pp. WA11.1-WA11.6, May 2003.

64. Paul Graham, Michael Caffrey, Michael Wirthlin, Eric Johnson, and Nathan Rollins, "Reconfigurable Computing in Space: From Current Technology to Reconfigurable Systems-On-a-Chip", *24th Annual IEEE Aerospace Conference*, Vol. 5, pp. 5:2399-5:2410, March 2003.

65. Nathan Rollins, Michael J. Wirthlin, Michael Caffrey, and Paul Graham, "Reliability of Programmable Input/Output Pins in the Presence of Configuration Upsets", *5th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, Paper C3, September 2002.

66. Michael Caffrey, Paul Graham, Eric Johnson, and Michael Wirthlin, "Single-Event Upsets in SRAM FPGAs", *5th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, Paper P8, September 2002.

Patents

67. Michael J. Wirthlin and Brad L. Hutchings, "Dynamically-Configurable Digital Processor Using Method for Relocating Logic Array Modules", U.S. Patent Number 6,173,434, January 2001.

Presentations and Posters

68. Brian Pratt, Michael Wirthlin, Michael Caffrey, Paul Graham, and Keith Morgan, "Analysis of SEU-induced Errors in an FPGA-based Digital Communications System", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* September 2008.

69. Patrick Ostler, Michael Caffrey, Derrick Gibelyou, Paul Graham, Keith Morgan, Brian Pratt, Heather Quinn, Michael Wirthlin, "FPGA System Error Rate Analysis for Harsh Radiation Environments", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* September 2008.

70. Brian Pratt, Michael Wirthlin, Paul Graham, Keith Morgan, and Severn Shelly, "Improving FPGA Reliability in Harsh Environments Using Triple-Modular Redundancy with More Frequent Voting", Military and Aerospace FPGA and Applications (MAFA), November 2007.

71. Jonathan Heiner, Nathan Collins, and Michael Wirthlin, "Correcting Single-Event Upsets Using Self-Hosting Partial Dynamic Reconfiguration", Military and Aerospace FPGA and Applications (MAFA), November 2007.

72. Michael Wirthlin, "Computing with FPGAs", Hybrid Computing Conference 2007, University of Utah.

73. M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Pritchard, P. Palazzari, G. Kuzmanov, "OpenFPGA CoreLib Core Library Interoperability Effort", Reconfigurable Systems Summer Institute, July 2007.

74. Michael Wirthlin, Dan McMurtrey, Brian Pratt and Keith Morgan, "A Comparison of TMR With Alternative Fault Tolerant Design Techniques for FPGAs", *2007 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, poster presentation, February 2007.

75. Joshua D. Engel, Keith S. Morgan, and Michael J. WirthlinPoster: "A Methodology for Estimating On-orbit Static Single Event Upset Rates Using CREME96", 9*th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2006.

76. Matthew French, Michael Wirthlin, and Paul Graham, Poster: "Reducing Power Consumption of Radiation Mitigated Designs for FPGAs", 9*th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2006.

77. Nathan Rollins and Michael J. Wirthlin, Poster: "Reducing Energy in FPGA Multipliers Through Glitch Reduction", *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.

78. Matthew French, Li Wang, Tyler Anderson, and Michael J. Wirthlin, Poster: "Integrated Tool Suite for Post Synthesis FPGA Power Consumption Analysis", *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.

79. Michael J. Wirthlin, invited presentation, "Reliable Spatial Computing", *1st Annual Distributed Embedded Computing Conference*, Sante Fe, NM, June 2005.

80. Michael J. Wirthlin, Invited Tutorial, "Evaluating Soft Errors in FPGAs", *IEEE International Reliability Physics Symposium*, April 2004.

81. Paul Graham, Michael Caffrey, Michael Wirthlin, D. Eric Johnson, and Nathan Rollins, Poster: "SEU Mitigation for Half-Latches in Xilinx Virtex FPGAs", *2003 IEEE Nuclear and Space Radiation Effects Conference*, June 2003.

82. Michael Wirthlin, D. Eric Johnson, Nathan Rollins, Paul Graham, and Michael Caffrey, Poster: "Validation of an FPGA Fault Simulator ", *2003 IEEE Nuclear and Space Radiation Effects Conference*, June 2003.

83. Michael J. Wirthlin, Trent Vandenberghe, and Devin Pratt , "JHDL Domain", presentation at the *5th Bi-annual Ptolemy mini-conference*, University of California at Berkeley, May 2003.

84. Michael J. Wirthlin, and Matthew Koecher , "JHDL Hardware Generation", presentation at the *5th Bi-annual Ptolemy mini-conference*, University of California at Berkeley, May 2003.

85. Michael J. Wirthlin, "The Effects of Upsets within the Configuration Memory of SRAM FPGAs", presentation at the *IEEE Microelectronics Reliability and Qualification Workshop*, December 2002.

86. Michael J. Wirthlin, Eric Johnson, and Michael Caffrey, "Single-Event Upset Simulation for Field Programmable Gate Arrays", presentation at the *2002 IEEE Nuclear and Space Radiation Effects Conference (NSREC 2002)*, 2002.

87. Michael J. Wirthlin, "Integrating the JHDL Design Environment into Ptolemy-II", presentation at the *4th Bi-annual Ptolemy mini-conference*, University of California, March 2001.

Externally Funded Contracts:

National Science Foundation CHREC Center:2010
Sponsors @ $35k each: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, National Instruments, L3 Communications, Rincon, NASA-Dryden, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/09-12/09, $280,000
"BYU Site for CHREC I/UCRC"

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 10/09-9/10, $48,000
"Non-Volatile Memory Review and Analysis – Contract Extension"

National Science Foundation CHREC Center:2009
Sponsors @ $35k each: Los Alamos National Laboratory (x2), Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, National Instruments, L3 Communications, Rincon, NASA-Dryden, SEAKR Corporation, and Xilinx Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/09-12/09, $350,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center:2008
Sponsors @ $35k each: Los Alamos National Laboratory (x2), Sandia National Laboratory, NASA GFSC, Lockheed Martin, National Instruments, L3 Communications, Rincon
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/08-12/08, $245,000
"Brigham Young University To Join the I/UCRC CHREC Center"

Defense Advanced Research Project Agency (DARPA)
PI: Mike Wirthlin, Co-PI: Brent Nelson, Brad Hutchings, 9/07-7/08, $348,000
"Future FPGA Design Methodologies and Tool Flows"

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 9/07-8/08, $108,711
"Non-Volatile Memory Review and Analysis"

National Science Foundation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/07-12/07, $10,000
"Brigham Young University To Join the I/UCRC CHREC Center"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/07-12/09, $300,000
"Automated Design Techniques for Improving FPGA Fault Tolerance"

Lockheed Martin CE&T
PI: Michael Wirthlin, 9/06-9/07, $50,000
"Dynamic Internal Reconfigurable Technology"

Naval Undersea Warfare Center (NUWC)
PI: Steve Shultz, Richard Selfridge, and Michael Wirthlin, 5/06-10/08, $355,657
"Harsh Environment D-fiber Sensors (HEDS)"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/06-9/06, $50,000
"Reliability Modeling of the Xilinx VirtexII and Virtex4 FPGAs"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/04-12/06, $270,000

"Improving the Reliability of FPGA Designs through Automated Design Hardening"

Xilinx Corporation
PI: Brent Neslon, Co-PI: Michael Wirthlin, 4/04-4/05, $80,000
"Pro-Media Processor Development Kit"

National Aeronautics and Space Administration (NASA), sub-contract through USC-ISI
Sub-contract PI: Michael Wirthlin, 5/03-4/06, $150,000
"Reconfigurable Hardware IN Orbit (RHINO)"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/02-12/03, $120,000
"Improving the Reliability of FPGA Designs Operating in a Space Environment"

Defense Advanced Research Projects Agency
PI: B. Hutchings, Co-PI: B. Nelson, M. Wirthlin, and D. Wilde, 1999-2002, $2,489,870
"Unified Debug Environment for Adaptive Computing Systems"

Internally Funded Projects:

Ira Fulton College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2005, $6,500
"Optimized Retiming and Operation Selection for Reconfigurable Data-Path Architectures"

Watson Embedded Systems Laboratory, Dept. of Electrical and Computer Engineering
M. Wirthlin, 2004-2005, $12,000
"High-Level Scheduling and Mapping Techniques for Reconfigurable Datapaths"

College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2000, $5,400
"Exploratory Research in Temporal Partitioning and Scheduling"

Student Graduates:

Welson Sun, Doctor of Philosophy (PhD), April 2008
"Using duplication with compare for on-line error detection in FPGA-based designs"

Dan L. McMurtrey, Masters of Science, December 2006
"Using duplication with compare for on-line error detection in FPGA-based designs"

Keith S. Morgan, Masters of Science, August 2006
"SEU-Induced Persistent Error Propagation in FPGAs"

D. Eric Johnson, Masters of Science, August 2005
"Estimating the Dynamic Sensitive Cross Section of FPGA Design Through Fault Injection"

Matthew R. Koecher, Masters of Science, December 2003
"Hardware Synthesis of Synchronous Data Flow Models"

Brian J. McMurtrey, Masters of Science, April 2003
"Approaches in Web Based Design and Evaluation of Digital Circuits"

Benjamin L. Bullough, Masters of Science, August 2002
"Analysis of Field-Programmable Gate Array Implementations of Constant Coefficient Finite Impulse Response Filters"

Wesley J. Landaker, Masters of Science, August 2002
"Using Hardware Context-Switching to Enable a Multitasking Reconfigurable Computer System"

Steven E. Morrison, Masters of Science, April 2001
"Design and Performance Analysis of a Configurable Hardware Solution of an Adaptive Automatic Target Recognition Algorithm"