Dr. Brent E. Nelson

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Education

PhD - Computer Science, University of Utah, 1984
MS - Computer Science, University of Utah, 1983
BS - Computer Science, University of Utah, 1981

Professional Experience

Department Chair, Department of Electrical and Computer Engineering, Brigham Young University June 2012 - present

BYU Site Co-Director, National Science Foundation Center for High-performance Reconfigurable Computing (CHREC), 2013-present.

Ira A. Fulton Chair in Globalization, Ira A. Fulton College of Engineering and Technology, Brigham Young University, 2010-2012.

Co-Director, National Science Foundation Center for High-performance Reconfigurable Computing (CHREC) and BYU CHREC Site Director, 2008-2012

Computer Engineering Program Head, Department of Electrical and Computer Engineering, Brigham Young University, May 2003-present

Professor, Department of Electrical and Computer Engineering, Brigham Young University September 1996-present

Visiting Scholar, Sanders Corporation, Nashua New Hampshire, May 1999 - August 1999

Department Chair, Department of Electrical and Computer Engineering, Brigham Young University August 1993 - October 1997

Associate Professor, Department of Electrical and Computer Engineering, Brigham Young University September 1990 - August 1996

Visiting Scholar, Intel Corporation, Hillsboro Oregon, May 1991 - August 1991

Director, Center for Parallel Supercomputing, Brigham Young University August 1990 - August 1991

Visiting Scholar, General Dynamics Corporation, San Diego California, May 1987 - August 1987

Assistant Professor, Department of Electrical and Computer Engineering, Brigham Young University October 1984 - August 1990

Professional Activities

Member – IEEE, ACM

Conference Organizing – Program Co-Chair, 2009 International Workshop on Field-Programmable Logic and Applications (FPL), Program Chair 2016 International Conference on Field Programmable Technology (ICFPT).

Current or Past Program Committees - High Performance Embedded Computing Workshop (HPEC), FPGA's for Custom Computing Machines (FCCM), International Conference on Field Programmable Technology (ICFPT), International Workshop on Field-Programmable Logic and Applications (FPL), Application-Specific Systems, Architectures and Processors (ASAP), Asia/South Pacific Design Automation Conference (ASPDAC)

Current or Past Referee/Reviewer – IEEE Transactions on VLSI Systems, IEEE Transactions on CAD, IEEE Transactions on Computers, National Science Foundation, Netherlands Organization for Scientific Research (NWO), Hong Kong Research Grants Council, Natural Sciences and Engineering Research Council of Canada, International Symposium on Circuits and Systems (ISCAS), High Performance FPGA/Reconfigurable Computing Workshop (HiPCRW), FCCM, FPGA, ICFPT, ASAP.

Keynotes and Invited Talks

1. "FPGA Design Productivity", ARC'2009, February 2009, Karlsruhe Germany.
2. "FPGA Design Productivity", International Conference on Field Programmable Technology (ICFPT'08), December 2008, Taipei Taiwan.
3. "FPGA Design Productivity: Existing Limitations and Root Causes and Future Research Approaches", National Aerospace and Electronics Conference (NAECON), Dayton Ohio, July 2008.
4. "FPGA Design Productivity: Existing Limitations and Root Causes and Future Research Approaches", ERSA'2008: The International Conference on Engineering of Reconfigurable Systems and Algorithms, Las Vegas Nevada, July 2008.
5. "Don't Look Back, The Best is Yet to Come… - The Future of Configurable Computing", ICFPT, Kitakyushu, Japan, December 2007.
6. "The Mythical CCM: In Search of Usable (and Reusable) FPGA-Based General Computing Machines", 17th IEEE Conference on Application-Specific Systems, Architectures, and Processors, Steamboat Springs Colorado, September 2006.
7. "The Design of an FPGA-Based MIMO Receiver: Architectural and Algorithmic Interactions", Asilomar Conference on Signals and Systems, Pacific Grove California, November 2006.
8. "Application Deployment on CCM's ", Asia Pacific Technology Forum (ICFPT), Hong Kong, December 2002.
9. "FPGA-Based High-Performance Reconfigurable Computing", High Performance Embedded Computing (HPEC), September 1998.

Book Chapters

1. Brent Nelson, Brad Hutchings, "The JHDL Design and Debug System", in Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation (Systems on Silicon), Scott Hauck and Andre DeHon editors, November 2007, pp. 255-273, ISBN: 0123705223.
2. Brad Hutching, Brent Nelson, "Implementing Applications With FPGAs", in Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation (Systems on Silicon), Scott Hauck and Andre DeHon editors, November 2007, pp. 439-452, ISBN: 0123705223.

Publications

3. Brad White, Brent Nelson, “TINCR - A Custom CAD Tool Framework For VIVADO”, 2014 International Conference on ReConFigurable Computing and FPGAs, Cancun Mexico, December 2014.
4. Christopher Lavin, Brent Nelson, Brad Hutchings, “Improving Clock-Rate of Hard-Macro Designs”, in Proceedings of the 2013 International Conference on Field-Programmable Technology (ICFPT 13), Kyoto Japan, December, 2013, DOI: 10.1109/FPL.2013.6645510.
5. Christopher Lavin, Brent Nelson, Brad Hutchings, “Impact of Hard Macro Size on FPGA Clock Rate and Place/Route Time”, in Proceedings of the 23rd International Conference on Field Programmable Logic and Applications (FPL), Porto Portugal, September, 2013, DOI: 10.1109/FPL.2013.6645510.
6. Travis Haroldsen, Brent Nelson, and Brad White, "Rapid FPGA Design Prototyping Through Preservation Of System Logic: A Case Study", in Proceedings of the 23rd International Conference on Field Programmable Logic and Applications (FPL), Porto Portugal, September, 2013, DOI: 10.1109/FPL.2013.6645539.
7. Yubo Li, Brent Nelson, Michael Wirthlin, “Reliability Models for SEC/DED Memory with Scrubbing in FPGA-based Designs”, IEEE Transactions on Nuclear Science, vol. 60, no. 4, April 2013, DOI: 10.1109/TNS.2013.2251902.
8. Kevin Ellsworth, Alex Harding, Colby Ballew, Travis Haroldsen, Michael Wirthlin, and Brent Nelson, Radiation Testing of FPGA-Based High-Speed Serial Communication, Proceedings of European Radiation Effects on Components and Systems Conference (RADECS), September 2012.
9. Yubo Li, Brent Nelson, Michael Wirthlin, “Reliability Models for SEC/DED Memory with Scrubbing in FPGA-based Designs”, Proceedings of European Radiation Effects on Components and Systems Conference (RADECS), September 2012.
10. Monreal, R.; Swift, G.; Wang, Y.C.; Wirthlin, M.; Nelson, B., Single Event Effect Rate Analysis and Upset Characterization of FPGA Digital Signal Processors, 2013 IEEE Radiation Effects Data Workshop (REDW), San Francisco CA, July 2012, DOI: 10.1109/REDW.2013.6658210.
11. Harding, A.; Ellsworth, K.; Nelson, B.; Wirthlin, M., Characterization and Mitigation of the MGT-Based Aurora Protocol in a Radiation Environment, 2013 IEEE Radiation Effects Data Workshop (REDW), San Francisco CA, July 2012, DOI: 10.1109/REDW.2013.6658186.
12. Subhrashanka Ghosh, Brent Nelson, “XDL-Based Module Generators for Rapid FPGA Design Implementation”, in Proceedings of the 21st International Conference on Field Programmable Logic and Applications (FPL'2011), Chania Greece, Sep. 2011.
13. Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson, Brad Hutchings, RapidSmith: Do-It-Yourself CAD Tools for Xilinx FPGAs, in Proceedings of the 21st International Conference on Field Programmable Logic and Applications (FPL'2011), Chania Greece, Sep. 2011.
14. Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson and Brad Hutchings, “HMFlow: Accelerating FPGA Compilation with Hard Macros for Rapid Prototyping”, in Proceedings of The 19th Annual IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM’11), Salt Lake City Utah, May 1-3, 2011.
15. Kevin Ellsworth, Travis Haroldsen, Brent Nelson, and Michael Wirthlin, “Dual Channel Architecture for Reliable FPGA high Speed Serial Links”, Proceedings of the 2011 IEEE Aerospace Conference, Big Sky, MT, March 5-12, 2011.
16. Yubo Li; Nelson, B.; Wirthlin, M.; , "Synchronization Techniques for Crossing Multiple Clock Domains in FPGA-Based TMR Circuits," Nuclear Science, IEEE Transactions on , vol.57, no.6, pp.3506-3514, Dec. 2010, doi: 10.1109/TNS.2010.2086075,
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5658028&isnumber=5657993

17. Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson and Brad Hutchings, “Rapid Prototyping Tools for FPGA Designs: RapidSmith”, in Proc. of International Conference on Field-Programmable Technology (FPT), Beijing, China, December 8-10, 2010.
18. Robert Todd, Michael Miles, Spencer Magleby, Brent Nelson, Randy Lewis, and Jim Nelson, “A Preliminary Report On Uniform Outcomes Assessment Of A College Wide Set Of International Programs”, Proc. Of ASEE 2010 Annual Conference & Exposition, Louisville KY, March, 2010.
19. Z.Y. Wei, D.J. Lee, B.E. Nelson, and J.K Archibald, “Hardware Friendly Vision Algorithms for Embedded Obstacle Detection Applications,” IEEE Transactions on Circuits and Systems for Video Technology, vol. 20/11, p. 1577-1589, November 2010.
20. M. Rice, B. Nelson, M. Padilla, and J. Havican, “On The Use of Rapid Prototyping for Designing PCM/FM Demodulators in FPGAs”, Proc. Of 2010 International Telemetering Conference (ITC), Las Vegas NV, Oct. 24-27, 2010.
21. Christopher Lavin, Marc Padilla, Subhrashankha Ghosh, Brent Nelson, Brad Hutchings, and Michael Wirthlin, “Using Hard Macros to Reduce FPGA Compilation Time”, in Proceedings of the 20th International Conference on Field Programmable Logic and Applications (FPL'2010), Aug. 31 - Sep. 2, 2010.
22. Adam Arnesen, Kevin Ellsworth, Derrick Gibelyou, Travis Haroldsen, Jared Havican, Marc Padilla, Brent Nelson, Michael Rice, and Michael Wirthlin, “Increasing Design Productivity Through Core Reuse, Meta-Data Encapsulation, and Synthesis”, in Proceedings of the 20th International Conference on Field Programmable Logic and Applications (FPL'2010), Aug. 31 - Sep. 2, 2010.
23. John Bodily, Brent Nelson, Zhaoyi Wei, Dah-Jye Lee, and Jeff Chase, “A Comparison Study On Implementing Optical Flow and Digital Communications on FPGAs and GPUs”, ACM Transactions on Reconfigurable Technology and Systems (TRETS) , Vol. 3, No. 2, May 2010, pp. 1-22.
24. D.J. Lee, P.C. Merrell, Z.Y. Wei, and B.E. Nelson, “Two-Frame Structure from Motion Using Optical Flow Probability Distributions for Unmanned Air Vehicle Obstacle Avoidance,” Machine Vision and Applications Journal, doi: 10.1007/s00138-008-0148-9, Vol. 3, pp. 229-240, April 2010.
25. Jon-Paul Anderson, Brent Nelson, Mike Wirthlin, "Using Statistical Models with Duplication and Compare for Reduced Cost FPGA Reliability", Proc. Of IEEE Aerospace Conference (AERO), Big Sky, MT, Mar. 6-13, 2010.
26. M. Rice, M. Padilla, and B. Nelson, "On FM Demodulators in Software-Defined Radios Using FPGAs," Proc. of Military Communications Conference (MILCOM), Boston, MA, Oct. 18-21, 2009
27. Hutchings, Brent Nelson, Stephen West, Reed Curtis, “Comparing Fine-Grained Performance on the Ambric MPPA Against an FPGA”, In Proceedings of the 19th International Conference on Field Programmable Logic and Applications (FPL'2009), Aug. 31 - Sep. 2 2009.
28. B. Hutchings, B. Nelson, S. West, and R. Curtis, "Implementing Optical Flow on the Ambric AM2045 MPAA," Proc. of 16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa, CA, Apr. 5-7, 2009.
29. D.J. Lee, P.C. Merrell, B.E. Nelson, and Z.Y. Wei, “Multi-Frame Structure from Motion using Optical Flow Probability Distributions,” Journal of Neurocomputing, vol. 72/4-6, p. 1032-1041, doi:10.1016/j.neucom.2008. 04.013, January 2009.
30. Z.Y. Wei, D.J. Lee, and B.E. Nelson, “Accurate Optical Flow Sensor for Obstacle Avoidance,“ Lecture Notes in Computer Science (LNCS), Part I, LNCS 5358, p. 240-247, International Symposium on Visual Computing (ISVC), Las Vegas, NV, U.S.A., December 1-3, 2008.
31. Z.Y. Wei, D.J. Lee, B.E. Nelson, and J.K. Archibald, “Real-time Accurate Optical Flow-based Motion Sensor,” IEEE International Conference on Pattern Recognition (ICPR), Tampa, FL, USA, December 8-11, 2008.

32. Brent E. Nelson, Brad L. Hutchings, and Michael J. Wirthlin. Design, Debug, Deploy: The Creation of Configurable Computing Applications. Journal of Signal Processing Systems, 53(1):187-196, November 2008.

33. Lavin, Christopher; Nelson, Brent; Palmer, Joseph; Rice, Michael, "An FPGA-ase Sace-time Coded Telemetry Receiver," IEEE National Aerospace and Electronics Conference, 2008 (NAECON 2008), vol., no., pp.250-256, 16-18 July 2008,
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4806555&isnumber=4806498

34. Brent Nelson, Michael Wirthlin, Brad Hutchings, Peter Athanas, Shawn Bohner, "Design Productivity for Configurable Computing", Proceedings of The International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'2008), Las Vegas, July 2008.

35. Z.Y. Wei, D.J. Lee, B.E. Nelson, J.K. Archibald, and B.B. Edwards, "FPGA-Based Embedded Motion Estimation Sensor," International Journal of Reconfigurable Computing, vol. 2008, Article ID 636145, 8 pages, doi:10.1155/2008/636145, July 2008.

36. J. Chase, B. Nelson, J. Bodily, Wei Z., and Lee D.J. Real-Time Optical Flow Calculations on FPGA and GPU Architectures: A Comparison Study. In Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM '08). IEEE Computer Society, IEEE Computer Society Press, April 2008, p. 173-182.

37. Z.Y. Wei, D.J. Lee, and B.E. Nelson, "A Hardware Friendly Adaptive Tensor-based Optical Flow Algorithm," Lecture Notes in Computer Science (LNCS), Part II, LNCS 4842, p. 43-51, International Symposium on Visual Computing (ISVC), Lake Tahoe, CA, U.S.A., November 26-28, 2007.

38. Z.Y. Wei, D.J. Lee, and B.E. Nelson, "FPGA-based Real-time Optical Flow Algorithm Design and Implementation," Journal of Multimedia, 2(5), p. 38-45, September 2007.

39. Z. Wei, D.J. Lee, B.E. Nelson, and M.A. Martineau. A Fast and Accurate Tensor-based Optical Flow Algorithm Implemented in FPGA. In Proceedings of the IEEE Workshop on Applications of Computer Vision (WACV 2007), pages 18-23, February 2007.

40. J.M. Palmer, M.D. Rice, and B.E. Nelson. A Low-Variance and Low- Complexity Carrier-Frequency-Offset Estimator Using Multiple Pilot Sequences. In Proceedings of MILCOM 2007, October 2007.

41. B. Nelson, M. Rice, and J. Palmer. The Design of an FPGA-Based MIMO Receiver: Architectural and Algorithmic Interactions. In Proceedings of the Asilomar Conference on Signals and Systems, November 2006.

42. K.D. Lillywhite, D.J. Lee, B.J. Tippetts, S.G. Fowers, A.W. Dennis, B.E. Nelson, and J.K. Archibald, "An Embedded Vision System for an Unmanned Four-rotor Helicopter," SPIE Optics East, Intelligent Robots and Computer Vision XXIV: Algorithms, Techniques, and Active Vision, vol. 6384, 63840G, Boston, MA, USA, October 1-4, 2006.

43. Brent E. Nelson. The Mythical CCM: In Search of Usable (and Reusable) FPGA-Based General Computing Machines. In Proceedings of 17th IEEE Conference on Application-Specific Systems, Architectures, and Processors, September 2006.

44. C. Hilton and B. Nelson. PNoC: A Flexible Circuit-Switched NoC for FPGA-Based Systems . IEE Proceedings - Computers and Digital Techniques, 153(3):181-188, May 2006.

45. C. Hilton and B. Nelson. A Circuit-Switched NOC for FPGA-Based Systems. In Proceedings of the 15th International Conference on Field Programmable Logic and Applications (FPL'2005), August 2005.

46. B. Catanzaro and B. Nelson. Higher Radix Floating-Point Representations for FPGA-Based Arithmetic. In Kenneth L. Pocek and Jeffrey M. Arnold, editors, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM '05). IEEE Computer Society, IEEE Computer Society Press, April 2005.

47. A. Poetter, J. Hunter, C. Patterson, P. Athanas, B. Nelson, and N. Steiner. JHDLBits: The Merging of Two Worlds. In Proceedings of the 14th International Conference on Field Programmable Logic and Applications (FPL'2004), August 2004.

48. J. Palmer and B. Nelson. A Parallel FFT Architecture for FPGAs. In Proceedings of the 14th International Conference on Field Programmable Logic and Applications (FPL'2004), pages 948-953, August 2004.

49. Brad L. Hutchings and Brent E. Nelson. GigaOp DSP on FPGA. The Journal of VLSI Signal Processing, 36(1):41-55, January 2004.

50. G. Ahlquist, B. Nelson, and M. Rice. Small and Fast Finite Field Multipliers for Field Programmable Gate Arrays (FPGAs). In Proceedings of the 11th Annual NASA Symposium on VLSI Design, May 2003.

51. X. J. Wang and B. Nelson. Tradeoffs of Designing Floating-Point Division and Square Root on Virtex FPGAs . In Kenneth L. Pocek and Jeffrey M. Arnold, editors, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM '03). IEEE Computer Society, IEEE Computer Society Press, April 2003.

52. A. Slade and B. Nelson. Reconfigurable Computing Application Frameworks . In Kenneth L. Pocek and Jeffrey M. Arnold, editors, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM '03). IEEE Computer Society, IEEE Computer Society Press, April 2003.

53. E. Roesler and B. Nelson. Debug Methods for Hybrid CPU/FPGA Systems. In Proceedings of The First IEEE International Conference on Field-Programmable Technology (FPT), pages 243-251, December 2002.

54. E. Roesler and B. Nelson. Novel Optimizations for Hardware Floating-Point Units in a Modern FPGA Architecture. In Proceedings of the 12th International Workshop on Field Programmable Logic and Applications (FPL'2002), pages 637-646, August 2002.

55. G. Ahlquist, B. Nelson, and M. Rice. Design and Synthesis of Small and Fast Finite Field Multipliers. In Proceedings of The 5th Annual Military and Aerospace Programmable Logic Device International Conference (MAPLD'2002), September 2002.

56. B. Nelson. Configurable Computing and Sonar Processing - Architectures and Implementations. In ASILOMAR 2001, November 2001.

57. B. Hutchings and B. Nelson. Giga Op DSP On FPGA. In Proceedings of ICASSP 2001, May 2001.

58. T. Wheeler, P. Graham, B. Nelson, and B. Hutchings. Using Design-Level Scan to Improve FPGA Design Observability and Controllability for Functional Verification. In Proceedings of the 11th International Workshop on Field Programmable Logic and Applications, volume 2147 of Lecture Notes in Computer Science, pages 483-492. Springer-Verlag, August/September 2001.

59. P. Graham, B. Nelson, and B. Hutchings. Instrumenting Bitstreams for Debugging FPGA Circuits. In Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'2001), April 2001.

60. B. Hutchings and B. Nelson. Unifying Simulation and Execution in a Design Environment for FPGA Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2(1):201-205, February 2001.

61. Brad Hutchings, Brent Nelson, and Michael J. Wirthlin. Designing and Debugging Custom Computing Applications. IEEE Design & Test of Computers, 17(1):20-28, January 2000.

62. B. Hutchings and B. Nelson. Using General-Purpose Programming Languages for FPGA Design. In Proceedings of the 37th Design Automation Conference, pages 561-566, June 2000.

63. S. Scalera, M. Falco, and B. Nelson. A Reconfigurable Computing Architecture for Microsensors. In Kenneth L. Pocek and Jeffrey M. Arnold, editors, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM '00), pages 59-67. IEEE Computer Society, IEEE Computer Society Press, April 2000.

64. P. Graham, B. Hutchings, and B. Nelson. Improving the FPGA Design Process Through Determining and Applying Logical-to-Physical Design Mappings. In Proceedings of the IEEE Symposium on Field Programmable Custom Computing Machines (FCCM'2000), April 2000.
65. G. Ahlquist, B. Nelson, and M. Rice. Optimal Finite Field Multipliers for FPGAs. In Proceedings of the 9th International Workshop on Field Programmable Logic and Applications (FPL'1999), pages 51-60, August 1999.
66. B. Hutchings, P. Bellows, J. Hawkins, S. Hemmert, B. Nelson, and M. Rytting. A CAD Suite for High-Performance FPGA Design. In K. L. Pocek and J. M. Arnold, editors, Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines, pages 12-24, Napa, CA, April 1999. IEEE Computer Society, IEEE.
67. P. Graham and B. Nelson. Reconfigurable Processors for High-Performance Embedded Digital Signal Processing. In Proceedings of the 9th International Workshop on Field Programmable Logic and Applications (FPL'1999), pages 1-10, August 1999.
68. G. Ahlquist, M. Rice, and B. Nelson. Error Control Coding in Software Radios: An FPGA Approach. IEEE Personal Communications, 6(4):35-39, August 1999.
69. Paul Graham and Brent Nelson. FPGA-Based Sonar Processing. In J. Cong and S. Kaptanoglu, editors, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, pages 201-208, Monterey, CA, February 1998. ACM SIGDA, ACM Press.
70. P. Graham and B. Nelson. Genetic Algorithms In Software and In Hardware | A Performance Analysis Of Workstation and Custom Computing Machine Implementations. In J. Arnold and K. Pocek, editors, Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, pages 216-225, Napa, CA, April 1996.
71. K. Grimsrud, J. Archibald, R. Frost, and B. Nelson. Locality as a Visualization Tool. IEEE Transactions on Computers, pages 1319-1326, November 1996.
72. G. Thompson, B. Nelson, and K. Flanagan. Transaction Processing Workloads - A Comparison to the SPEC Benchmarks Using Memory Hierarchy Performance Analysis. In Proc. of Int. Workshop on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS'96), pages 152-156, February 1996.
73. K. Flanagan, B. Nelson, and G. Thompson. Incomplete Traces and Trace-Driven Simulation. In Proc. of Int. Workshop on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS'96), pages 37-43, February 1996.
74. P. Graham and B. Nelson. A Hardware Genetic Algorithm for the Travelling Salesman Problem on SPLASH 2. In W. Moore and W. Luk, editors, Field-Programmable Logic and Applications, pages 352-361, Oxford, England, August 1995. Springer.
75. A. Severson and B. Nelson. Throughput in a Counterflow Pipeline Processor. Computer Architecture News, April 1995.
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77. B. Nelson, R. Jones, and D. Kirkpatrick. Simulation Event Pattern Checking with PROTO. In Proc. of the International Conference on Simulation and Hardware Description Languages, pages 115-121, January 1994.
78. K. Grimsrud, J. Archibald, M. Ripley, K. Flanagan, and B. Nelson. BACH - A Hardware Monitor for Tracing Microprocessor-Based Systems. Microprocessors and Microsystems, 17(8):443-459, October 1993.
79. R. Smith, J. Archibald, and B. Nelson. Evaluating Performance of Prefetching Second Level Caches. Performance Evaluation Review - ACM Sigmetrics, 20(4):32-44, May 1993.

80. K. Grimsrud, J. Archibald, and B. Nelson. Multiple Prefetch Adaptive Disk Caching. IEEE Transactions on Knowledge and Data Engineering, 5(1):88-103, February 1993.
81. K. Flanagan, B. Nelson, J. Archibald, and K. Grimsrud. Incomplete Trace Data and Trace-Driven Simulation. In Proc. of Int. Workshop on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS'93), pages 203-209, January 1993.
82. K. Grimsrud, J. Archibald, R. Frost, and B. Nelson. Estimation of Simulation Error Due to Trace Inaccuracies. In Proc. of 26th Asilomar Conference on Signals, Systems and Computers, October 1992.
83. K. Flanagan, B. Nelson and J. Archibald, and K. Grimsrud. BACH: BYU Address Collection Hardware; The Collection of Complete Traces. In Proc. of 6th Int. Conf. on Modeling Techniques and Tools for Computer Performance Evaluation, pages 51-65, September 1992.
84. L. Salmon, J. Archibald, and B. Nelson. Impact of Advanced Packaging Technologies on Computer Architecture. In IEEE Computer Society Workshop, February 1992.
85. B. Nelson, J. Archibald, and K. Flanagan. Performance Analysis of Inclusion Effects in Multi-Level Multiprocessor Caches. In Proc. of the Third IEEE Symp. on Parallel and Distributed Processing, pages 513-516, December 1992.
86. D. Boggs, J. Archibald, and B. Nelson. Accurate Performance Evaluation of Systems with Two-Level Caches using Trace-Driven Simulation. In Proc. of the Fourth ISMM Int. Conf. on Parallel and Distributed Computing and Systems, pages 240-244, October 1991.
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88. S. Son, B. Nelson, and J. Archibald. Efficient Utilization of Distributed Workstation Resources. In Proc. of 9th Annual Conf. on University Programs in Computer-Aided Engineering, Design and Manufacturing (UPCAEDM 91), pages 121-126, May 1991.
89. T. Li, S. Zhao, and B. Nelson. Parallel Iterative Deepening for Optimization. In Proc. of Parallel and Distributed Computing of Systems, 1990.
90. T. Li, B. Nelson, and K. Flanagan. CMOS Implementation of a Correlator for Delta-Modulated Signals. International Journal of Electronics, 67(2):215-220, August 1989.
91. T. Li and B. Nelson. Designing Systolic Processors Using SYSIM2. Progress in Computer-Aided VLSI Design, 3, 1989.
92. J. Lawlor, B. Nelson, and J. Archibald. CSIM: A Discrete Simulation Package for C. In Proceedings of the 1989 Summer Computer Simulation Conference, pages 20-24, July 1989.
93. J. Flanagan, D.Morrell, R. Frost, C. Read, and B. Nelson. Vector Quantization Codebook Generation Using Simulated Annealing. In Proceedings of International Conference on Acoustics, Speech, and Signal Processing, May 1989.
94. J. Flanagan and B. Nelson. Processor Design Using Path Programmable Logic. In Proceedings of 1988 IEEE International Conference on Computer Design: VLSI in Computers & Processors, October 1988.
95. T. Li, B. Nelson, K. Flanagan, and C. Read. A Multiprogrammed Parallel Architecture For Digital Signal Processing. In Proceedings of the 1987 IEEE International Conference on Acoustics, Speech, and Signal Processing, April 1987.
96. B. Nelson, D. Morrell, C. Read, and K. Smith. The PPL Integrated Circuit Design Methodology. Computer-Aided Design, 18(9):481-488, November 1986.
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98. T. Li and B. Nelson. Parallel Processing of Linear Quadtrees. In Proceedings of the First International Conference on Future Advances in Computing, February 1986.

99. L. Hollaar, B. Nelson, T. Carter and R. Lorie. The Structure And Operation of a Relational Database System in a Cell-Oriented Integrated Circuit Design System. In Proceedings of the 21st Design Automation Conference, pages 117-125, June 1984.

100. E. Organick, T. Carter, M Maloney, A. Davis, A. Hayes, D. Klass, G. Lindstrom, B. Nelson, and K. Smith. Transforming An Ada Program Unit to Silicon and Verifying Its Behavior in an Ada Environment: A First Experiment. IEEE Software, pages 31-49, January 1984.

101. B. Nelson, K. Smith, and T. Carter. Cost Effective VLSI Design System. In IEEE International Symposium on Circuits and Systems, May 1983.

102. K. Smith, B. Nelson, and K. Stevens. Student-Designed VLSI at the University of Utah. In Proceedings of the IEEE 2nd CAD/CAM Workshop, December 1983.

103. K. Smith, B. Nelson, T. Carter, and A. Hayes. Computer-aided Design of Integrated Circuits Using Path-Programmable Logic. In IEEE Electro 83 Professional Program Session Record, April 1983.

104. T. Carter, K. Smith, B. Nelson, A. Hayes, and D. Fisher. Path-Programmable Logic and the Use of Cadds2/VLSI. In Proceedings of the Fourth Annual International Computervision User Conference, pages 523-528, September 1982.