JEFFREY GOEDERS

Assistant Professor, Brigham Young University
Department of Electrical and Computer Engineering

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EDUCATION

PhD	The University of British Columbia, Vancouver, Canada Dept. of Electrical and Computer Engineering *"Techniques for Enabling In-System Observation-based Debug of High-Level Synthesis Circuits on FPGAs"*	2012–2016
MASc	The University of British Columbia, Vancouver, Canada Dept. of Electrical and Computer Engineering *"Power Estimation for Diverse FPGA Architectures"*	2010–2012
BASc, Honors	University of Toronto, Toronto, Canada Computer Engineering	2007–2010

PROFESSIONAL EXPERIENCE

Brigham Young University 2016—Present
Assistant Professor of Electrical and Computer Engineering

PUBLICATIONS

Book Chapters: *(2 published)*

1. **Jeffrey Goeders**, Graham M. Holland, Lesley Shannon, and Steven J.E. Wilton, "Systems-on-Chip on FPGAs," chapter in FPGAs for Software Programmers, Springer, 2016.
2. Andrew Canis, Jongsok Choi, Blair Fort, Bain Syrowik, Ruo Long Lian, Yu Ting Chen, Hsuan Hsiao, **Jeffrey Goeders**, Stephen Brown, and Jason Anderson, "LegUp high-level synthesis," chapter in FPGAs for Software Programmers, Springer, 2016.

Peer-Reviewed Journal Publications: *(6 published)*

3. Al-Shahna Jamal, Eli Cahill, **Jeffrey Goeders**, and Steven JE Wilton, "Fast Turnaround HLS Debugging using Dependency Analysis and Debug Overlays," in Transactions on Reconfigurable Technology and Systems, vol. 13, no. 1, pp. 1-26, Feb 2020.
4. Benjamin James, Heather Quinn, Michael Wirthlin, and **Jeffrey Goeders**, "Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms, "in Transactions on Nuclear Science (TNS), vol. 67, no. 1, pp. 321-327, Jan 2020.
5. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, "Microcontroller Compiler-Assisted Software Fault Tolerance," in Transactions on Nuclear Science (TNS), vol. 66, no. 1, pp. 223-232, Jan 2019.

6. **Jeffrey Goeders**, and Steven J.E. Wilton, "Signal-Tracing Techniques for In-System FPGA Debugging of High-Level Synthesis Circuits," in Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 36, no. 1, pp. 83-96, Jan 2017.
7. **Jeffrey Goeders** and Steven J.E. Wilton, "Power Aware Architecture Exploration for Field Programmable Gate Arrays," in Journal of Low Power Electronics (JOLPE), vol. 10, no. 3, pp. 297-312, Sep. 2014.
8. Jason Luu, **Jeffrey Goeders**, Michael Wainberg, Andrew Somerville, Thien Yu, Konstantin Nasartschuk, Miad Nasr, Sen Wang, Tim Liu, Nooruddin Ahmed, Kenneth B Kent, Jason Anderson, Jonathan Rose, and Vaughn Betz, "VTR 7.0: Next Generation Architecture and CAD System for FPGAs," in Transactions on Reconfigurable Technology and Systems (TRETS), vol 7, no. 2, pp. 6:1–30, Jul. 2014.

Peer-Reviewed International Conference Publications: *(18 published)*

Note: Conferences which were refereed by abstract, or had acceptance rates close to 100% are not listed in this section. Most relevant conferences in this field are the "4-Fs": Int'l Symposium on Field-Programmable Gate Arrays (FPGA), Int'l Conf. on Field-Programmable Technology (FPT), Int'l Conf. on Field-Programmable Logic and Applications (FPL), Int'l Conf. on Field-Config. Custom Computing Machines (FCCM). Acceptance rates for these conferences are regularly below 30%.

9. Matthew Ashcraft and **Jeffrey Goeders**, "Synchronizing On-Chip Software and Hardware Traces for HLS-Accelerated Programs," in International Conference on Field Programmable Technology (FPT), Dec 2019.
10. Wesley Stirk and **Jeffrey Goeders**, "Implementation and Design Space Exploration of a Turbo Decoder in High-Level Synthesis," in International Conference on Reconfigurable Computing and FPGAs (ReConFig), Dec 2019.
11. Daniel Holanda Noronha, Ruizhe Zhao, Zhiqiang Que, **Jeffrey Goeders**, Wayne Luk and Steve Wilton, "An Overlay for Rapid FPGA Debug of Machine Learning Applications," in International Conference on Field Programmable Technology (FPT), Dec 2019.
12. Daniel Holanda Noronha, Ruizhe Zhao, **Jeffrey Goeders**, Wayne Luk, and Steven J.E. Wilton, "On-chip FPGA Debug Instrumentation for Machine Learning Applications," in International Symposium on Field-Programmable Gate Arrays (FPGA), pp. 110-115, Feb 2019.
13. Matthew Ashcraft and **Jeffrey Goeders**, "Unified On-Chip Software and Hardware Debug for HLS-Accelerated Programs," in International Conference on Field Programmable Technology (FPT), pp. 354-357, Dec 2018.
14. Al-Shahna Jamal, **Jeffrey Goeders** and Steve Wilton, "An FPGA Overlay Architecture Supporting Rapid Implementation of Functional Changes during On-Chip Debug," in International Conference on Field Programmable Logic and Applications (FPL), Aug. 2018.
15. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, "Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ," in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2018.
16. Al-Shahna Jamal, **Jeffrey Goeders,** and Steven J.E. Wilton, "Architecture Exploration for HLS-Oriented FPGA Debug Overlays," in International Symposium on Field-Programmable Gate Arrays (FPGA), Feb 2018.
17. Pavan Kumar Bussa, **Jeffrey Goeders**, and Steven JE Wilton, "Accelerating in-system FPGA debug of high-level synthesis circuits using incremental compilation techniques," in International Conference on Field Programmable Logic and Applications (FPL), Sep 2017.
18. **Jeffrey Goeders**, "Enabling Long Debug Traces of HLS Circuits Using Bandwidth-Limited Off-Chip Storage Devices," in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017.

19. **Jeffrey Goeders**, and Steven J.E. Wilton, "Quantifying observability for in-system debug of high-level synthesis circuits," in International Conference on Field Programmable Logic and Applications (FPL), pp. 1–11, Aug. 2016.
20. **Jeffrey Goeders**, and Steven J.E. Wilton, "Using Round-Robin Tracepoints to Debug Multithreaded HLS Circuits on FPGAs," in International Conference on Field Programmable Technology (FPT), Dec. 2015.
21. **Jeffrey Goeders**, and Steven J.E. Wilton, "Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs," in International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 127–134, May 2015. **BEST PAPER AWARD.**
22. **Jeffrey Goeders**, and Steven J.E. Wilton, "Effective FPGA Debug for High-Level Synthesis Generated Circuits," in International Conference on Field Programmable Logic and Applications (FPL), pp. 1–8, Sep. 2014.
23. Eddie Hung, **Jeffrey Goeders**, and Steven J.E. Wilton, "Faster FPGA Debug: Efficiently Coupling Trace Instruments with User Circuitry," in International Symposium on Applied Reconfigurable Computing (ARC), pp. 73–84, Apr. 2014.
24. **Jeffrey Goeders**, and Steven J.E. Wilton, "VersaPower: Power Estimation for Diverse FPGA Architectures," in International Conference on Field Programmable Technology (FPT), pp. 229–234, Dec. 2012.
25. Jonathan Rose, Jason Luu, Chi Wai Yu, Opal Densmore, **Jeffrey Goeders**, Andrew Somerville, Kenneth B. Kent, Peter Jamieson, and Jason Anderson, "The VTR Project: Architecture and CAD for FPGAs from Verilog to Routing," in International Symposium on Field Programmable Gate Arrays (FPGA), pp. 77 – 86, Feb. 2012.
26. **Jeffrey Goeders**, Guy Lemieux, and Steven J.E. Wilton, "Deterministic Timing-Driven Parallel Placement by Simulated Annealing Using Half-Box Window Decomposition," in International Conference on Reocnfigurable Computing and FPGAs (ReConFig), pp. 41–48, Dec. 2011.

Peer-Reviewed International Workshop Publications *(1 published)***:**

27. Adam Hastings, Sean Jensen, **Jeffrey Goeders**, and Brad Hutchings, "Using Physical and Functional Comparisons to Assure 3rd-Party IP for Modern FPGAs," in International Verification and Security Workshop (IVSW), Jul. 2018.

Peer-Reviewed International Poster Presentations:

28. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, "Microcontroller Compiler-Assisted Software Fault Tolerance," in Nuclear and Space Radiation Effects Conference (NSREC), Jul. 2018.

TALKS

Invited Talks:

1. **Jeffrey Goeders,** Tanner Gaskin, and Brad Hutchings, "Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ," at Xilinx Inc., Boulder, CO, May 2018.
2. **Jeffrey Goeders**, and Steven J.E. Wilton, "In-System FPGA Debugging of High-Level Synthesis Circuits," at Intel Programmable Solutions Group, Toronto, ON, Canada, Apr. 2016.
3. **Jeffrey** Goeders, and Steven J.E. Wilton, "Techniques for In-System FPGA Debugging of High-Level Synthesis Circuits," at University of Toronto, Toronto, ON, Canada, Apr. 2016.
4. **Jeffrey Goeders**, and Steven J.E. Wilton, "Effective FPGA Debug for High-Level Synthesis Generated Circuits," at Xilinx Inc., San Jose, CA, USA, Apr. 2015.

5. **Jeffrey Goeders,** and Steven J.E. Wilton, "Effective FPGA Debug for High-Level Synthesis Generated Circuits," at Altera Corp., Toronto, ON, Canada, Jan. 2015.

Conference Talks:

6. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, "Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ," in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2018.
7. **Jeffrey Goeders**, "Enabling Long Debug Traces of HLS Circuits Using Bandwidth-Limited Off-Chip Storage Devices," at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017.
8. **Jeffrey Goeders**, and Steven J.E. Wilton, "Quantifying observability for in-system debug of high-level synthesis circuits," at International Conference on Field Programmable Logic and Applications (FPL), Aug. 2016.
9. **Jeffrey Goeders**, and Steven J.E. Wilton, "Using Round-Robin Tracepoints to Debug Multithreaded HLS Circuits on FPGAs," at International Conference on Field Programmable Technology (FPT), Dec. 2015.
10. **Jeffrey Goeders**, and Steven J.E. Wilton, "Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs," at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2015.
11. **Jeffrey Goeders**, and Steven J.E. Wilton, "Effective FPGA Debug for High-Level Synthesis Generated Circuits," at International Conference on Field Programmable Logic and Applications (FPL), Sep. 2014.
12. **Jeffrey Goeders**, Guy Lemieux, and Steven J.E. Wilton, "Deterministic Timing-Driven Parallel Placement by Simulated Annealing Using Half-Box Window Decomposition," at International Conference on Reconfigurable Computing and FPGAs (ReConFig), Dec. 2011.

Workshop Talks:

13. Adam Hastings, Sean Jensen, **Jeffrey Goeders**, and Brad Hutchings, "Using Physical and Functional Comparisons to Assure 3rd-Party IP for Modern FPGAs," in International Verification and Security Workshop (IVSW), Jul. 2018.
14. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, "Automated Data Flow Protection for Software Fault Tolerance on Microcontrollers," in Silicon Errors in Logic – System Effects (SELSE), Apr. 2018.
15. **Jeffrey Goeders**, and Steven J.E. Wilton, "VersaPower: Power Estimation for Diverse FPGA Architectures," at Cascadia: A joint workshop of UBC, SFU, and UWash on FPGA Research, SFU, Aug. 2012.

Artifact Demonstrations:

16. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, "Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ," at Xilinx Developer Forum (XDF), Oct 2018.
17. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, "Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ," at International Symposium on Field-Programmable Custom Computing Machines (FCCM), Oct 2018.
18. **Jeffrey Goeders**, and Steven J.E. Wilton, "HLS-Scope: Debug Hardware Like it's Software. Effective Source-Level Debugging of High-Level Synthesis Generated Circuits," at Innovation 360: Symposium and Exposition on Micro-Nano Technologies and Systems, Sep. 2015.
19. **Jeffrey Goeders**, and Steven J.E. Wilton, "HLS-Scope: FPGA Debug for High-Level Synthesis", at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2015.
20. **Jeffrey Goeders**, and Steven J.E. Wilton, "HLS-Scope: FPGA Debug for High-Level Synthesis", at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2014.

TEACHING EXPERIENCE

Instructor

ECEN 220: Fundamentals of Digital Systems (Spring 2019, Fall 2019)
ECEN 330: Intro to Embedded System Programming (Fall 2016, Fall 2017, Fall 2018)
ECEN 522R: High-Level Digital Design Automation (Winter 2017)
ECEN 625: Compilation Strategies for High-Performance Programs (Winter 2019)
ECEN 629: Reconfigurable Computing Systems (Winter 2018, Winter 2020)

Teaching Assistant (2011-2016)

EECE 381: Computer Systems Design Studio (7 appointments)
EECE 465: Microcomputer Systems Design (1 appointment)
EECE 353: Digital Systems Design (3 appointments)
EECE 259: Introduction to Microcomputers (2 appointments)

COURSE DEVELOPMENT

ECEN 427: Embedded System Design (BYU)

- Developed major revisions to the lab content of the class in conjunction with the instructor, Brad Hutchings.
- New lab content focused on development for Linux embedded systems
- New labs give students a full-stack experience: creating a new digital circuit IP, integrating it into a Linux system, developing a Linux kernel driver, and finally integrating it into application code.

ECEN 522R: High-Level Digital Design Automation (BYU)

- Major revisions of existing course to introduce new assignments, lecture material, current research topics, and hands-on experience with major commercial tools.
- Developed four new assignments which give students experience with commercial designs, high-level synthesis algorithms, large open-source tools, including the LLVM compiler infrastructure.

EECE 381: Computer Systems Design Studio (UBC)

- Co-developed with Professor Steve Wilton at The University of British Columbia.
- Project-based course designed to give students real-world technical project skills. Students work in groups to identify a real-world market, identify constraints and requirements, plan project milestones, implement hardware and software, and present and report on their accomplishments.
- Technical topics: Rapid development of configurable hardware systems using commercial tools (Quartus/Qsys), embedded software development (FPGAs, Raspberry Pi, ARM), mobile applications (Android), and the integration of such systems.

EMPLOYMENT EXPERIENCE

Teaching Assistant 2011–2016
Dept. of Electrical and Computer Engineering, The University of British Columbia

EDA Software Developer (Internship) 2013
Blackcomb Design Automation, Vancouver, BC, Canada

Firmware Developer (Internship) 2010
PMC-Sierra, Burnaby, BC, Canada

Undergraduate Researcher, High-Performance Computing Lab 2009
University of Toronto, Toronto, ON, Canada

Software and Database Developer 2006–2009
Bombardier Aerospace, Toronto, ON, Canada

GOOGLE SCHOLAR PROFILE SUMMARY

Citations: 792
h-index: 9
i10-index: 9

PROFESSIONAL ACTIVITIES

Member of IEEE and ACM

Information Director (2018 – Present)
ACM Transactions on Reconfigurable Technology and Systems (TRETS)

Technical Program Committee Member
International Symposium on Field-Programmable Gate Arrays (FPGA)
- 2017 – Present (4 years)

International Conference on Field-Programmable Technology (FPT)
- 2016 – Present (4 years)

International Conference on Field-Programmable Custom Computing Machines (FCCM)
- 2018, 2020 (2 years)

Reviewer
ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- 2016 – Present

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- 2016 – Present

IEEE Transactions on Nuclear Science (TNS)
- 2018 – Present

IEEE Transactions on Computers (TC)
- 2019 – Present

ACM Transactions on Architecture and Code Optimization (TACO)
- 2017

International Journal of Reconfigurable Computing
- 2016

SOFTWARE ARTIFACTS

1. COAST (COmpiler-Assisted Software fault Tolerance) 2017–2018
   - Open-source package of software compiler passes for the LLVM compiler
   - Provide automated DWC or TMR protection transformation for arbitrary software programs.
   - https://github.com/byuccl/coast

2. LegUp 4.0 Debugger 2012–2016
   - LegUp is an open-source, academic high-level synthesis tool developed at the University of Toronto, downloaded by over 1500 research groups around the world.
   - My contribution to the project is an open-source debugger tool, HLS-Scope, which allows for debugging HLS circuits in-system while executing on an FPGA.
   - http://legup.eecg.utoronto.ca/docs/4.0/debug.html

3. Verilog-to-Routing (VTR) Project Contributions 2010–2012
   - The VTR project is world-wide collaborative effort among multiple research groups to provide an open-source framework for conducting FPGA architecture and CAD research and development.
   - My primary contribution is a power estimation tool, integrated into the VPR tool, which provides power estimates of user described FPGA architectures.
   - https://github.com/verilog-to-routing/vtr-verilog-to-routing