G. Scott Lloyd

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Education

Ph.D. – Computer Science, Brigham Young University, 2011
M.S. – Computer Science, Brigham Young University, 1985
B.S. – Chemistry, Brigham Young University, 1982

Teaching and Mentoring Experience

Electrical and Computer Engineering Dept., Brigham Young University, Provo, UT, 2020-present
Associate Professor

- EC EN 220 – Fundamentals of Digital Systems
- EC EN 224 – Introduction to Computer Systems
- EC EN 323 – Computer Organization
- EC EN 330 – Introduction to Embedded System Programming
- EC EN 390 – Junior Team Design Project
- EC EN 521 – Introduction to Algorithm Design
- EC EN 528 – High Performance Parallel Computing
- Capstone Coach – Mentor students through completion of industry supplied projects
  - Trusted and Assured FPGA-based Cryptographic Accelerators, 2022-2023,
    Jacob Burtenshaw, Sara Divingnzzo, Alek Farmer, Noah Hanks, Kaden Hardy, Kepa Zubeldia
  - SDR Network of RF Signal Emulators, 2021-2022,
    Tom Bates, Ben Karlinsey, Erik Pedersen, Jason Thomason
  - Photonic Doppler Velocimetry (PDV) Frequency Analysis, 2020-2021,
    Davin Fish, Bryan Henningson, Christopher Krueger, Sharisse Poff, Craig Roundy, Colin White

Lawrence Livermore National Laboratory, Livermore, CA
Mentor Summer Students – Advise in novel methods for advanced memory system evaluation

- Logan Moody, JMU – Viability of hardware accelerated floating-point compression, 2019
- Joshua Landgraf, UT Austin – Memory trace compression, 2018
- Joshua Landgraf, UT Austin – Simulating a near memory key/value accelerator, 2017
- Riju John Xavier, UF – Virtual memory translation for processing in memory, 2016
- Chris Hajas, UF – Emulating in-memory data reorganization for HPC, 2015
- Kevin Cheng, UF – An emulation framework for tracing near memory computation, 2014
- Adam Crume, UCSC – Dataflow LINPACK, 2012

Computer Science Dept., Brigham Young University, Provo, UT
Teaching Assistant CS 484 – Parallel Processing, Winter 2010

- Teach two class periods on MapReduce

Computer Science Dept., Brigham Young University, Provo, UT
Instructor CS 235 – Data Structures and Algorithms, Summer 2007

- Lecture and prepare presentation slides, work with teaching assistants

Research Experience

Lawrence Livermore National Laboratory, Livermore, CA, 2011-2020

Computer Scientist

- Implement ZFP floating-point compression in SystemC
- Develop a universal number (unum) floating-point library
- Research advanced memory systems
- Develop an FPGA-based memory subsystem emulator
- Submit patent application "Near-Memory Data Reorganization Engine"
- Characterize the Micron Hybrid Memory Cube

Brigham Young University, Provo, UT, 2005-2011

Research Assistant

- Investigate FPGA acceleration of biological sequence analysis

Professional Experience

MicroWorks, Boise, ID, 2003-2005

Senior Software Engineer

- Provide contract services with HP, and Agilent
- Debug laser printer firmware under test
- Verify and test ASIC designs with FPGA emulator

Micron Technology, Boise, ID, 2000-2003

Software Engineer

- Research processor-in-memory (PIM) architectures using embedded DRAM
- Write proposals for PIM architecture and software development tool suite
- Develop ANSI 'C' compiler and assembler for PIM architecture (VLIW)
- Implement convolution and DCT benchmarks on PIM system

GE Medical Systems (OEC), Salt Lake City, UT, 1999-2000

Lead Software Engineer

- Lead the design and integration of image guided surgery (IGS) with fluoroscope
- Write software development plan for integrated IGS/fluoroscope
- Submit patent disclosure; US patent 6,823,207; European patent 01307077.6-1522
- Implement fast bitmap rotation algorithm

Alta Technology Corp. (became Linux Networx), Sandy, UT, 1989-1999

Co-Founder/V.P. Software

- Design and engineer the founding hardware and software products
- Investigate new parallel processing and communication technology
- Design cluster management system with temperature monitoring and power sequencing
- Adapt BIOS and NT HAL code for Digital Alpha motherboard
- Develop boot loader & EEPROM utilities

Computer System Architects, Provo, UT, 1987-1988

Software Engineer

- Develop multi-tasking, communications library for parallel, 32-bit microprocessor
- Implement multi-processor, photo-realistic, 3-D graphics, ray tracing demonstration

Modula Corporation, Provo, UT, 1984-1986

Software Engineer

- Collaborate on design and development of printed circuit layout package

Professional Training

"Effective Modern C++" – Jon Kalb (Scott Meyers material), 2019
"Entrepreneurship Academy" – UC Davis, 2016
"Software Project Survival" – Steve McConnell, 2000
"Shlaer-Mellor Object Oriented Analysis" – Leon Starr, 1999

Awards

DDS&T Excellence in Publication Award, LLNL, 2019
CASC Spot Award for work on LiME, LLNL, 2019
United States Patent 9,965,187 Issued May 8, 2018
Best Paper Award, MemSys, 2015
Global Security Gold Award, 2014
Best Paper Award, ReConFig, 2008
United States Patent 6,823,207 Issued November 23, 2004
Outstanding Undergraduate Student Award in analytical chemistry
Phi Eta Sigma

Publications

Z. Wu, M. Gokhale, S. Lloyd and H. Patel, "SCCL: An Open-Source SystemC to RTL Translator," *Proceedings of FCCM*, IEEE, 1-10, May 2023. doi:10.1109/FCCM57271.2023.00012

M. Barrow, Z. Wu, S. Lloyd, M. Gokhale, H. Patel and P. Lindstrom, "ZHW: A Numerical CODEC for Big Data Scientific Computation," *Proceedings of ICFPT*, IEEE, 1-9, December 2022. doi:10.1109/ICFPT56656.2022.9974258

A. Jain, S. Lloyd and M. Gokhale, "Performance Assessment of Emerging Memories Through FPGA Emulation," *IEEE Micro*, vol. 39:1, 8-16, January/February 2019. doi:10.1109/MM.2018.2877291

S. Lloyd and M. Gokhale, "Design Space Exploration of Near Memory Accelerators," *Proceedings of MemSys*, ACM, 218-220, October 2018. doi:10.1145/3240302.3240428

A. Jain, S. Lloyd and M. Gokhale, "Microscope on Memory: MPSoC-enabled Computer Memory System Assessments," *Proceedings of FCCM*, IEEE, 173-180, May 2018. doi:10.1109/FCCM.2018.00035

P. Lindstrom, S. Lloyd and J. Hittinger, "Universal Coding of the Reals: Alternatives to IEEE Floating Point," *Proceedings of CoNGA*, ACM, 5:1-5:14, March 2018. doi:10.1145/3190339.3190344

S. Lloyd and M. Gokhale, "Near Memory Key/Value Lookup Acceleration," *Proceedings of MemSys*, ACM, 26-33, October 2017. doi:10.1145/3132402.3132434

S. Lloyd and M. Gokhale, "Evaluating the Feasibility of Storage Class Memory as Main Memory," *Proceedings of MemSys*, ACM, 437-441, October 2016. doi:10.1145/2989081.2989118

M. Gokhale, S. Lloyd and C. Macaraeg, "Hybrid Memory Cube Performance Characterization on Data-centric Workloads," *Proceedings of IA^3*, ACM, 7:1-7:8, November 2015. doi:10.1145/2833179.2833184

M. Gokhale, S. Lloyd and C. Hajas, "Near Memory Data Structure Rearrangement," *Proceedings of MemSys*, ACM, 283-290, October 2015. doi:10.1145/2818950.2818986 (Best Paper)

S. Lloyd and M. Gokhale, "In-memory Data Rearrangement for Irregular, Data Intensive Computing," *IEEE Computer*, vol. 48, 18-25, August 2015. doi:10.1109/MC.2015.230

S. Ames, D. Hysom, S. Gardner, S. Lloyd, M. Gokhale and J. Allen, "Scalable Metagenomic Taxonomy Classification Using a Reference Genome Database," *Bioinformatics*, vol. 29, 2253-2260, 2013. doi:10.1093/bioinformatics/btt389

S. Lloyd and Q. Snell, "Accelerated Large-Scale Multiple Sequence Alignment," *BMC Bioinformatics*, 12:466, 2011. doi:10.1186/1471-2105-12-466 (Highly Accessed)

S. Lloyd and Q. Snell, "Hardware Accelerated Sequence Alignment with Traceback," *International Journal of Reconfigurable Computing*, vol. 2009, Article ID 762362, 10 pages, 2009. doi:10.1155/2009/762362

S. Lloyd and Q. Snell, "A Packet-Switched Network Architecture for Reconfigurable Computing," *ACM Trans. Embedd. Comput. Syst.*, 9, 1, Article 7, 17 pages, October 2009. doi:10.1145/1596532.1596539

Program Committees

International Conference on Supercomputing, 2019
Memory Centric High Performance Computing, 2018-2019
International Parallel and Distributed Processing Symposium, 2018
International Symposium on Memory Systems, 2016-2018
Biotechnology and Bioinformatics Symposium, 2011-2016

Open Source Contributions

ZHW – ZFP Hardware Implementation. A floating-point compression algorithm in hardware. http://github.com/LLNL/zhw

LiME – Logic in Memory Emulator. Memory subsystem emulator with benchmark applications. http://github.com/LLNL/lime, and http://github.com/LLNL/lime-apps

PERM – Persistent Memory Library. Adds checkpointing and memory-mapped heap files to the jemalloc allocator. http://computing.llnl.gov/projects/memory-centric-architectures/perm

Unum – Universal Number Library. Implements a new variable precision floating-point format. http://github.com/LLNL/unum