Michael J. Wirthlin

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Department of Electrical and Computer Engineering
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Education:

Ph.D. Brigham Young University, Provo, UT - Electrical and Computer Engineering
Dissertation: Improving Functional Density Through Run-Time Circuit Reconfiguration
August 1997

B.S. Brigham Young University, Provo, UT - Electrical and Computer Engineering
August 1992, Suma Cum Laude with University Honors
Honors Thesis: A Quantitative Study of RISC Pipelining Techniques Using Custom Software Simulation Tools

Areas of Specialization:

FPGA Reliability
Digital Circuit Design
FPGA Circuit Design
High-Level Synthesis
Single-Event Effects Testing
Computer System Reliability
Reconfigurable Computing Architectures
Application-Specific Computing Architectures
Reliable Computing
Fault-Tolerant Computing

Professional Experience:

Assistant, Associate, and Full Professor (1999 – present)
Dept. of Electrical and Computer Engineering, Brigham Young University, Provo, UT

Intellectual Property Legal Consultant (2004-2005, 2011-2013, 2015-2016)
Pia Anderson Dorius Reynard & Moss, Salt Lake City, UT
Maschoff Brennan, Salt Lake City, UT
Workman Nydegger, Salt Lake City, UT
Irell and Manella, LLP, Los Angeles, CA

- Review patents in computer architecture, hardware design, and software systems
- Testify in patent litigation and intellectual property disputes

Staff Engineer (1997-1998)
National Semiconductor, Architecture Laboratory, Santa Clara, CA

- Investigate and develop system design methodologies for single-chip systems
- Create system performance modeling for embedded system on chip architectures

Design Engineer (1992-1994)
National Technology Incorporated, Salt Lake City, UT

- FPGA design of digital sound products
- Configurable computing architecture development

Controls Engineer, Co-Op (1990-1991)
Saturn Corporation, Lost Foam and Vehicle Systems Operations, Spring Hill, TN

- PLC programmer for automobile manufacturing facility

Professional Activities

Senior Member of the IEEE, member of IEEE Computer Society
Member of the Association for Computing Machinery (ACM), Tau Beta Pi
Steering Committee for the International IEEE Symposium on Field-Programmable Custom Computing Machines (2011-present)
Program Session Organizer, IEEE Nuclear and Space Radiation Effects Conference, 2017
Chair and organizer of the Soft-Errors and Programmable Logic (SEPL) Workshop, 2016
Publications Chair for the Military Aerospace Programmable Logic Devices (MAPLD) Workshop, 2014
Program Co-Chair for the International Conference on Reconfigurable Computing and FPGAs (ReConFig 2013-2014),
Technical Co-Chair for the Military Aerospace Programmable Logic Devices (MAPLD) Workshop, April 2013
General Chair for the International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2011)
Technical Program Co-Chair for the International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2010)
Technical program committee and publicity chair for International Conference on Field Programmable Logic and Applications (FPL 2008-2009)
Reviewer for *IEEE Transactions on VLSI Systems*, *Kluwer Journal of VLSI Signal Processing*, *IEEE Computer Magazine*, ACM Design Automation Conference, IEEE Symposium on Field-Programmable Custom Computing Machines, IEEE Transactions on Computers, and the International Symposium on Signal Processing and its Applications (ISSPA).
Review panelist for the National Science Foundation
Technical program committee for ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, International conference on Engineering of Reconfigurable Systems and Algorithms, and International Conference on Military and Aerospace Programmable Logic Devices (MAPLD).
Special session organizer (Reconfigurable System on Chip Architectures), International conference on Engineering of Reconfigurable Systems and Algorithms (2004)
Member of ACM/SIGDA DAC PhD forum organizing committee (2002-2004)

Educational Responsibilities

Department Associate Chair (2021 – Present)
Department ABET and Assessment Coordinator (2013 – 2021)
Department graduate coordinator (2006 – 2010)
University Sailing Club Advisor (2004 – 2009)

Awards:

Ira Fulton College of Engineering and Technology Excellence in Research Award, 2017
Ira Fulton College of Engineering and Technology Excellence in Citizenship Award, 2010
Outstanding Faculty Award, Dept. of Electrical and Computer Engineering, 2007
Faculty advisor to 3rd place at IEEE Computer Society International Design Competition, 2001

Courses Taught:

ECEN 220/224: Introductory Digital Design and State Machines
ECEN 320: Advanced Digital Design
ECEN 323: Computer Organization
ECEN 427: Embedded Systems
ECEN 490: Senior Project (Computer System Design Project, FPGA Software Radio Project)
ECEN 521: Introduction to Algorithm Design
ECEN 523: Computer System Reliability
ECEN 528: Advanced Computer Architecture
ECEN 625: Synthesis and Optimization of Digital Circuits
ECEN 523: Computer System Reliability

Courses Developed:

Computer Organization: Developed a new sequence of digital design laboratories leading students through the design of a simplified MIPs microprocessor.
Introduction to Digital Systems Laboratory: Developed a new sequence of twelve digital design laboratories based on the most recent design tools and digital logic systems.
Computer System Reliability: Developed a new three credit hour graduate course that includes reliability modeling concepts and fault tolerant computer system design techniques.
Advanced Digital Design Course: Developed a new five credit hour junior level digital design course to include relevant topics and more advanced material.
Advanced Digital Design Laboratory: Initiated the use of FPGAs in undergraduate teaching laboratories. Organized laboratory sequence for students to design and test a simple 16-bit processor.
Synthesis and Optimization of Digital Circuits: Introduced a new graduate course on digital circuit synthesis with an emphasis on scheduling and resource sharing.
Computer Systems Senior Project: Introduced a new senior project involving the specification, design, and testing of a complete computer system (hardware and software). Students taking this class participated in the IEEE Computer Society International Design Competition (CSIDC) and placed 3rd in the 2001 finals in Washington D.C.

Publications:

Journal Publications

1. Andrew M. Keller and Michael J. Wirthlin. "The Impact of Terrestrial Radiation on FPGAs in Data Centers". *ACM Trans. Reconfigurable Technol. Syst.* 15, 2, Article 12 (June 2022), 21 pages. DOI: 10.1145/3457198.
2. A. Pérez-Celis, C. Thurlow and M. Wirthlin, "Identifying Radiation-Induced Micro-SEFIs in SRAM FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 10, pp. 2480-2487, Oct. 2021, doi: 10.1109/TNS.2021.3108572.
3. A. Pérez-Celis, C. Thurlow and M. Wirthlin, "Emulating Radiation-Induced Multicell Upset Patterns in SRAM FPGAs With Fault Injection," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 8, pp. 1594-1599, Aug. 2021, doi: 10.1109/TNS.2021.3071704
4. A. M. Keller and M. J. Wirthlin, "Partial TMR for Improving the Soft Error Reliability of SRAM-Based FPGA Designs," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 1023-1031, May 2021, doi: 10.1109/TNS.2021.3070856
5. A. E. Wilson, S. Larsen, C. Wilson, C. Thurlow and M. Wirthlin, "Neutron Radiation Testing of a TMR VexRiscv Soft Processor on SRAM-Based FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 1054-1060, May 2021, doi: 10.1109/TNS.2021.3068835
6. F. Libano, P. Rech, B. Neuman, J. Leavitt, M. Wirthlin and J. Brunhaver, "How Reduced Data Precision and Degree of Parallelism Impact the Reliability of Convolutional Neural Networks on FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 865-872, May 2021, doi: 10.1109/TNS.2021.3050707
7. B. James, M. Wirthlin and J. Goeders, "Investigating How Software Characteristics Impact the Effectiveness of Automated Software Fault Tolerance," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 1014-1022, May 2021, doi: 10.1109/TNS.2021.3073259
8. A.E. Wilson, C. Thurlow, and M. Wirthlin, "Fault injection testing of fault tolerant RISC-V soft processors on Xilinx SRAM-based FPGAs," Journal of Radiation Effects Research Research and Engineering (JRERE), vol. 39, no. 1, pp. 317–322, Apr. 2021.
9. F. Libano, P. Rech, B. Neuman, J. Leavitt, M. Wirthlin and J. Brunhaver, "How Reduced Data Precision and Degree of Parallelism Impact the Reliability of Convolutional Neural Networks on FPGAs," in *IEEE Transactions on Nuclear Science*, doi: 10.1109/TNS.2021.3050707.

10. F. Libano, B. Wilson, M. Wirthlin, P. Rech and J. Brunhaver, "Understanding the Impact of Quantization, Accuracy, and Radiation on the Reliability of Convolutional Neural Networks on FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 67, no. 7, pp. 1478-1484, July 2020, doi: 10.1109/TNS.2020.2983662.
11. B. James, H. Quinn, M. Wirthlin and J. Goeders, "Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms", in *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, 321-327, Jan. 2020, doi: 10.1109/TNS.2019.2959975
12. M. J. Cannon, A. M. Keller, C. A. Thurlow, A. Pérez-Celis and M. J. Wirthlin, "Improving the Reliability of TMR with Non-Triplicated I/O on SRAM FPGAs", in *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 312-320, Jan. 2020, doi: 10.1109/TNS.2019.2956473
13. A. Pérez-Celis and M. J., "Statistical Method to Extract Radiation-Induced Multiple-Cell Upsets in SRAM-based FPGAs", in *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 50-56, Jan. 2020. doi: 10.1109/TNS.2019.2955006
14. P. Walton, J. Cannon, B. Damitz, T. Downs, D. Glick, J. Holtom, N. Kohls, A. Laraway, I. Matheson, J. Redding, C. Robinson, J. Ryan, N. Stoddard, J. Willis, K. Warnick, M. Wirthlin, D. Wilde, B. Iverson, and D. Long, "Passive CubeSats for remote inspection of space vehicles", in *Journal of Applied Remote Sensing*, vol. 13, no. 3, 2019. https://doi.org/10.1117/1.JRS.13.032505
15. M. J. Cannon, A. M. Keller, H. C. Rowberry, C. A. Thurlow, A. Pérez-Celis and M. J. Wirthlin, "Strategies for Removing Common Mode Failures From TMR Designs Deployed on SRAM FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 207-215, Jan. 2019. doi: 10.1109/TNS.2018.2877579
16. F. Libano, B. Wilson, J. Anderson, M. J. Wirthlin, C. Cazzaniga, C. Frost, P. Rech, "Selective Hardening for Neural Networks in FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 216-222, Jan. 2019. doi: 10.1109/TNS.2018.288446
17. M. Bohman, B. James, M. J. Wirthlin, H. Quinn and J. Goeders, "Microcontroller Compiler-Assisted Software Fault Tolerance, " in *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 223-232, Jan. 2019.
18. A. M. Keller, T. A. Whiting, K. B. Sawyer and M. J. Wirthlin, "Dynamic SEU Sensitivity of Designs on Two 28-nm SRAM-Based FPGA Architectures, " in *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 280-287, Jan. 2018. doi: 10.1109/TNS.2017.2772288
19. M. Brusati, A. Camplani, M. Cannon, H. Chen, M. Citterio, M. Lazzaroni, H. Takai, M. Wirthlin, "Mitigated FPGA design of multi-gigabit transceivers for application in high radiation environments of High Energy Physics experiments," *Measurement,* vol. 108, pp. 171-192, October 2017.
20. Aaron Stoddard, Aaron Gruwell, and Michael Wirthlin, "A Hybrid Approach to FPGA Configuration Scrubbing in High-Radiation Environments", *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 497-503, Jan. 2017.
21. Andrew Keller and Michael Wirthlin, "Benefits of Complementary SEU Mitigation for the LEON3 Soft Processor on SRAM-based FPGAs", *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 519-528, Jan. 2017.
22. M. Citterio, A. Camplani, M. Cannon, H. Chen, K. Chen, B. Deng, C. Liu, C. Meroni, J. Kierstead, H. Takai, M. Wirthlin, and J. Ye, "Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 824, pp. 270-271, July 11, 2016. doi:10.1016/j.nima.2015.11.033
23. N.A. Dodds, M.J. Martinez, P.E. Dodd, M.R. Shaneyfelt, F.W. Sexton, J.D. Black, D.S. Lee, S.E. Swanson, B.L. Bhuva, K.M. Warren, R.A. Reed, J. Trippe, B.D. Sierawski, R.A. Weller, N. Mahatme, N.J., Gaspard, T. Assis, R. Austin, S.L. Weeden-Wright, L.W. Massengill, G. Swift, M. Wirthlin, M. Cannon, R. Liu, L. Chen, A.T. Kelly, P.W. Marshall, M. Trinczek, E.W. Blackmore, S.-J. Wen, R. Wong, B. Narasimham, J.A. Pellish, and H. Puchner "The Contribution of Low-Energy Protons to the Total On-Orbit SEU Rate," *IEEE Transactions on Nuclear Science* , vol. 62, no. 6, pp. 2440–2451, Dec. 2015. (**Best Paper Award**)
24. D.S. Lee, G.M. Swift, M.J. Wirthlin, and J. Draper, "Addressing Angular Single-Event Effects in the Estimation of On-Orbit Error Rates," *IEEE Transactions on Nuclear Science,* vol.62, no.6, pp. 2563-2569, Dec. 2015.
25. M. Cannon, M. Wirthlin, A. Camplani, M. Citterio, and C. Meroni, "Evaluating Xilinx 7 Series GTX Transceivers for Use in High Energy Physics Experiments Through Proton Irradiation," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2695-2702, Dec. 2015.
26. H. Quinn, W.H. Robinson, P. Rech, M. Aguirre, A. Barnard, M. Desogus, L. Entrena, M. Garcia-Valderas, S.M. Guertin, D. Kaeli, F. Lima Kastensmidt, B.T. Kiddie, A. Sanchez-Clemente, M. Sonza Reorda, L. Sterpone, M. Wirthlin, "Using Benchmarks for Radiation Testing of Microprocessors and FPGAs," *IEEE Transactions on Nuclear Science,* vol.62, no.6, pp.2547-2554, Dec. 2015.
27. H. Quinn, and M. Wirthlin, "Validation Techniques for Fault Emulation of SRAM-based FPGAs," in *IEEE Transactions on Nuclear Science,* vol. 62, no. 4, pp.1487-1500, Aug. 2015.

28. M. Wirthlin, "High-Reliability FPGA-Based Systems: Space, High-Energy Physics, and Beyond," in *Proceedings of the IEEE*, vol.103, no.3, pp.379-389, March 2015.
29. Heather Quinn, Diane Roussel-Dupre, Mike Caffrey, Paul Graham, Michael Wirthlin, Keith Morgan, Anthony Salazar, Tony Nelson, Will Howes, Eric Johnson, Jon Johnson, Brian Pratt, Nathan Rollins, and Jim Krone, "The Cibola Flight Experiment," *ACM Trans. Reconfigurable Technol. Syst.* Volume 8, Issue 1, Article 3 (March 2015), 22 pages. 2015 (**Best article of 2015 award**).
30. M. Wirthlin, D. Lee, G. Swift, H. Quinn, "A Method and Case Study on Identifying Physically Adjacent Multiple-Cell Upsets Using 28-nm, Interleaved and SECDED-Protected Arrays," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp.3080-3087, Dec. 2014
31. Michael Wirthlin, Helio Takai, and Alex Harding, "Soft Error rate estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter", *IOP Science Journal of Instrumentation*, Vol. 9, No. C01025, January 2014.
32. Quinn, H.; Graham, P.; Morgan, K.; Baker, Z.; Caffrey, M.; Smith, D.; Wirthlin, M.; Bell, R., "Flight Experience of the Xilinx Virtex-4, " Nuclear Science, IEEE Transactions on, vol. 60, no. 4, pp. 2682-2690, Aug. 2013.
33. Michael Wirthlin, "FPGAs operating in a radiation environment: lessons learned from FPGAs in space", *IOP Science Journal of Instrumentation*, Vol. 8, No. C02020, February 2013.
34. Brian Pratt, Megan Fuller, Michael Rice, and Michael Wirthlin, "Reduced-Precision Redundancy for Reliable FPGA Communications Systems in High-Radiation Environments", *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 49, No. 1, pp. 369—379, January 2013.
35. Brian Pratt, Megan Fuller, and Michael Wirthlin, "Reduced-Precision Redundancy on FPGAs", *International Journal of Reconfigurable Computing*, Vol. 2011, 12 pages, Oct. 2011.
36. Yubo Li, Brent Nelson, and Michael Wirthlin, "Synchronization Techniques for Crossing Multiple Clock Domains in FPGA-Based TMR Circuits", *IEEE Transactions on Nuclear Science*, Vol. 57, No. 6, pp. 3506 - 3514, December 2010.
37. A. Propst, K. Peters, M. A. Zikry, S. Schultz, W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, "Assessment of damage in composite laminates through dynamic, full-spectral interrogation of fiber Bragg grating sensors", *Smart Materials and Structures*, Vol 19, Structures and Materials, p. 1-11, January 2010.
38. Patrick Ostler, Michael P. Caffrey, Derrick Gibelyou, Paul S. Graham, Keith S. Morgan, Brian H. Pratt, Heather M. Quinn, and Michael J. Wirthlin, "SRAM FPGA Reliability Analysis for Harsh Radiation Environments", *IEEE Transactions on Nuclear Science (NSREC)*, Vol. 56, No. 6, pp. 3519-3526, December 2009.
39. Heather Quinn, Paul Graham, Michael Wirthlin, Brian Pratt, Keith Morgan, Michael Caffrey, and Jim Krone, "A Test Methodology for Determining Space-Readiness of Xilinx SRAM-based FPGA Devices and Designs", *IEEE Transactions on Instrumentation and Measurement*, Vol. 58, No. 10, pp. 3380-3395, October 2009.
40. S. Schultz, W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, A. Propst, M. Zikry and K. Peters, "Full-spectrum interrogation of fiber Bragg grating sensors for dynamic measurements in composite laminates," *Smart Materials and Structures*, vol. 18, p. 115015, Sept. 2009.
41. Brian Pratt, Michael Caffrey, James F. Carroll, Paul Graham, Keith Morgan, and Michael Wirthlin, "Fine-Grain SEU Mitigation for FPGAs Using Partial TMR", *IEEE Transactions on Nuclear Science*, Vol. 55, No. 4, pp. 2274-2280, August 2008.
42. M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Pritchard, P. Palazzari, G. Kuzmanov, "OpenFPGA CoreLib Core Library Interoperability Effort", *Journal of Parallel computing*, Vol. 34, No. 4-5, pp. 231-244. 2008.
43. Brent E. Nelson, Brad L. Hutchings, and Michael J. Wirthlin, "Design, Debug, Deploy: The Creation of Configurable Computing Applications", *Journal of Signal Processing Systems*, Vol. 53, No. 1-2, pp. 187-196. 2008.
44. Keith Morgan, Daniel McMurtrey, Brian Pratt, and Michael Wirthlin, "A Comparison of TMR With Alternative Fault-Tolerant Design Techniques for FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 54, No. 6, Part 1, pp. 2065 - 2072, December 2007.
45. Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer, "FPGA Pipeline Synthesis Design Exploration Using Module Selection and Resource Sharing", *IEEE Transactions on Computer Aided Design*, Vol. 26, No. 2, pp. 254-265, February 2007.
46. Maya Gokhale, Paul Graham, Michael Wirthlin, D. Eric Johnson, and Nathaniel Rollins, "Dynamic Reconfiguration for Management of Radiation-Induced Faults in FPGAs", *International Journal of Embedded Systems*, Vol. 2, No. 1/2, pp. 28-38, 2006.
47. Keith Morgan, Michael Caffrey, Paul Graham, Eric Johnson, Brian Pratt, and Michael Wirthlin, "SEU-Induced Persistent Error Propagation in FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 52, No. 6, Part 1, pp. 2438 - 2445, December 2005.

48. D. Eric Johnson, Michael Caffrey, Paul Graham, Nathan Rollins, and Michael Wirthlin, "Accelerator Validation of an FPGA SEU Simulator", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 6, pp. 2147-2157, December 2003.
49. Paul Graham, Michael Caffrey, D. Eric Johnson, Nathan Rollins, and Michael Wirthlin, "SEU Mitigation for Half-Latches in Xilinx Virtex FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 6, pp. 2139-2146, December 2003.
50. Michael J. Wirthlin, "Constant Coefficient Multiplication Using Look-up Tables", *Journal of VLSI Signal Processing*, Vol. 36, pp. 7-15, 2004.
51. Edward A. Lee, Stephen Neuendorffer, and Michael J. Wirthlin, "Actor-Oriented Design of Embedded Hardware and Software Systems", Invited paper to the *Journal of Circuits, Systems, and Computer,* Vol. 12, No. 3, pp. 231-260, June 2003.
52. Michael J. Wirthlin and Brian McMurtrey, "Web-Based IP Evaluation and Distribution Using Applets", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems,* Vol. 22, No. 8, pp. 985-994, August 2003.
53. B. L. Hutchings, B. Nelson and M. J. Wirthlin, "Designing and Debugging Custom Computing Applications", *IEEE Design and Test of Computers*, Vol. 17, No. 1, pp. 20-28, January 2000.
54. M. J. Wirthlin and B.L. Hutchings, "Improving Functional Density Using Run-Time Circuit Reconfiguration", *IEEE Transactions on VLSI Systems*, vol. 6, no. 2, pp. 247-256, 1998.

Book Chapters

1. Alex Harding and Michael J. Wirthlin "Hybrid Configuration Scrubbing for Xilinx Series-7 FPGAs," Chapter 6 of FPGAs and Parallel Architectures for Aerospace Applications, pp. 61-74, Springer, 2016.
2. Nathan Harward, Michael Gardiner, Luke Hsiao, and Michael J. Wirthlin "A Fault Injection System for Measuring Soft Processor Design Sensitivity on Virtex-5 FPGAs," Chapter 7 of FPGAs and Parallel Architectures for Aerospace Applications, pp. 91-101, Springer, 2016.
3. Heather M. Quinn, Keith S. Morgan, Paul S. Graham, James B. Krone, Michael P. Caffrey, Kevin Lundgreen, Brian Pratt, David Lee, Gary M. Swift, Michael J. Wirthlin "Assuring Robust Triple-Modular Redundancy Protected Circuits in SRAM-Based FPGAs," Chapter 8 of Ionizing Radiation Effects in Electronics: From Memories to Imagers, CRC Press, pp. 195-228, 2015.
4. Keith S. Morgan, Los Alamos National Laboratory, James Carroll, Michael Caffrey, Derrick Gibelyou, Paul Graham, William Howes, Jonathan Johnson, Daniel McMurtrey, Patrick Ostler, Brian Pratt, Heather Quinn, Michael Wirthlin, "Fault Tolerance Techniques and Reliability Modeling for SRAM-based FPGAs", Chapter in Radiation Effects in Semiconductors: Devices, Circuits, and Systems, CRC Press, 2010.

Conference Publications, Full Paper Peer Review

1. A. E. Wilson and M. Wirthlin, "Fault Injection of TMR Open Source RISC-V Processors using Dynamic Partial Reconfiguration on SRAM-based FPGAs," *2021 IEEE Space Computing Conference (SCC)*, 2021, pp. 1-8, doi: 10.1109/SCC49971.2021.00008.
2. M. J. Cannon, A. M. Keller, A. Pèrez-Celis and M. J. Wirthlin, "Modeling Common Cause Failures in Systems with Triple Modular Redundancy and Repair," *2020 Annual Reliability and Maintainability Symposium (RAMS)*, Palm Springs, CA, USA, 2020, pp. 1-6, doi: 10.1109/RAMS48030.2020.9153662.
3. A. Keller, J. Anderson, M. Wirthlin, S. Wen, R. Fung and C. Chambers, "Using Partial Duplication With Compare to Detect Radiation-Induced Failure in a Commercial FPGA-Based Networking System," 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2020, pp. 1-6, doi: 10.1109/IRPS45951.2020.9128839.
4. D. Skouson, A. Keller, and M. Wirthlin, "Netlist Analysis and Transformations Using SpyDrNet", in Proceedings of the 19th Python in Science Conference (SciPy 2020), July 2020, pp. 40-47, doi: 10.25080/Majora-342d178e-006
5. C. Thurlow, H. Rowberry and M. Wirthlin, "TURTLE: A Low-Cost Fault Injection Platform for SRAM-based FPGAs," *2019 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, Cancun, Mexico, Feb. 2020. pp. 1-8. doi: 10.1109/ReConFig48160.2019.8994782
6. A. E. Wilson and M. Wirthlin, "Reconfigurable Real-Time Video Pipelines on SRAM-based FPGAs," *2019 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, Cancun, Mexico, Feb. 2020. doi: 10.1109/ReConFig48160.2019.8994814

7. A. Keller and M. Wirthlin, "Single-Event Characterization of a Stratix® 10 FPGA Using Neutron Irradiation," *2019 IEEE Radiation Effects Data Workshop*, pp. 1-6, November 2019. doi: 10.1109/REDW.2019.8906534
8. Andrew Wilson and Michael J. Wirthlin, "Neutron Radiation Testing of Fault Tolerant RISC-V Soft Processor on Xilinx SRAM-based FPGAs", 2019 IEEE Space Computing Conference (SCC), pp. 25-23, October 2019.
9. D. Glick, J. Grigg, B. Nelson and M. Wirthlin, "Maverick: A Stand-Alone CAD Flow for Partially Reconfigurable FPGA Modules," 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 9-16, June 2019.
10. Andrew Keller and Michael J. Wirthlin, "Impact of Soft Errors on Large-Scale FPGA Cloud Computing", *2018 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2018)*, pp. 272-281, February 2019.
11. J. D. Anderson, J. C. Leavitt and M. J. Wirthlin, "Neutron Radiation Beam Results for the Xilinx UltraScale+ MPSoC," *2018 IEEE Nuclear & Space Radiation Effects Conference (NSREC 2018)*, Waikoloa Village, HI, 2018, pp. 1-7. doi: 10.1109/NSREC.2018.8584297
12. D. S. Lee, M. King, W. Evans, M. Cannon, A. Pérez-Celis, J. Anderson, M. Wirthlin and W. Rice, "Single-Event Characterization of 16 nm FinFET Xilinx UltraScale+ Devices with Heavy Ion and Neutron Irradiation, " *2018 IEEE Nuclear & Space Radiation Effects Conference (NSREC 2018)*, Waikoloa Village, HI, 2018, pp. 1-8. doi: 10.1109/NSREC.2018.8584313
13. M. Cannon, A. Keller and M. Wirthlin, "Improving the Effectiveness of TMR Designs on FPGAs with SEU-Aware Incremental Placement," *2018 IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Boulder, CO, 2018, pp. 141-148. doi: 10.1109/FCCM.2018.00031
14. B. Hutchings and M. Wirthlin, "Rapid implementation of a partially reconfigurable video system with PYNQ", *Proceedings of the 27th International Conference on Field Programmable Logic and Applications (FPL-2017)*, September 2017, pp. 1-8, DOI: 10.23919/FPL.2017.8056845
15. David S. Lee, Gary Swift, and Michael Wirthlin, "An Analysis of High-Current Events Observed on Xilinx 7-Series and UltraScale Field- Programmable Gate Arrays," *2016 IEEE Radiation Effects Data Workshop (REDW)*, pp.1-5, Dec. 2016.
16. Ammon Gruwell, Peter Zabriskie, and Michael Wirthlin, "High-Speed FPGA Reliability Testing Over JTAG", *IEEE AUTOTESTCON 2016*, September, 2016, pp. 1-8, DOI: 10.1109/AUTEST.2016.7589601
17. Aaron Stoddard and Michael Wirthlin, "High-speed PCAP configuration scrubbing on Zynq-7000 All Programmable SoCs", *Proceedings of the 26th International Conference on Field Programmable Logic and Applications (FPL-2016)*, September 29, 2016, pp. 1-8, DOI: 10.1109/FPL.2016.7577301
18. Luke Newmeyer, Michael J. Wirthlin, Doran Wilde, and Brent Nelson, "Efficient Processing of Phased Array Radar in Sense and Avoid Application Using Heterogeneous Computing", *Proceedings of the 26th International Conference on Field Programmable Logic and Applications (FPL-2016)*, September 29, 2016, pp. 1-8, DOI: 10.1109/FPL.2016.7577322
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2. Brent Nelson, Michael Wirthlin, Kevin Ellsworth, Alex Harding, Colby Ballew, and Travis Haroldsen, “Radiation Testing of FPGA-Based High-Speed Serial Communication”, Proceedings of European Radiation Effects on Components and Systems Conference (RADECS), September 2012.
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11. Brian Pratt, D. Eric Johnson, Michael J. Wirthlin, Michael Caffrey, Keith Morgan, and Paul Graham, “Improving FPGA Design Robustness with Partial TMR”, *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.

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Patents

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Presentations and Posters

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2. Helio Takai and Michael Wirthlin, "Accelerator Radiation Environment and the Use of FPGAs in those Environments", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2015.
3. Michael Wirthlin, "Accelerator Radiation Environment and the Use of FPGAs in those Environments", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2015.
4. Michael Wirthlin, "Neutron Radiation Test Results of the Linux Operating System Executing within the CHREC Space Processor (CSP)", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2015.
5. M. Wirthlin, "A Unique Fault Injection System for Estimating MicroBlaze Design Reliability on Xilinx V5QV FPGAs", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2014.
6. P. Gauvin, J. Urriste, C. Wilson, C. Morales, A. Stoddard, A. Wilson, A. George, G. Crum, M. Wirthlin, H. Lam, "CSP: A Multifaceted Hybrid System for Space Computing", *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2014.
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14. Jonathan Heiner, Nathan Collins, and Michael Wirthlin, "Correcting Single-Event Upsets Using Self-Hosting Partial Dynamic Reconfiguration", Military and Aerospace FPGA and Applications (MAFA), November 2007.
15. Michael Wirthlin, "Computing with FPGAs", Hybrid Computing Conference 2007, University of Utah.
16. M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Pritchard, P. Palazzari, G. Kuzmanov, "OpenFPGA CoreLib Core Library Interoperability Effort", Reconfigurable Systems Summer Institute, July 2007.
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18. Joshua D. Engel, Keith S. Morgan, and Michael J. WirthlinPoster: "A Methodology for Estimating On-orbit Static Single Event Upset Rates Using CREME96", 9*th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2006.
19. Matthew French, Michael Wirthlin, and Paul Graham, Poster: "Reducing Power Consumption of Radiation Mitigated Designs for FPGAs", 9*th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2006.
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25. Michael Wirthlin, D. Eric Johnson, Nathan Rollins, Paul Graham, and Michael Caffrey, Poster: "Validation of an FPGA Fault Simulator ", *2003 IEEE Nuclear and Space Radiation Effects Conference*, June 2003.
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Externally Funded Contracts and Gifts:

National Science Foundation SHREC Center: 2021
Sponsors: BAE, Raytheon, L3Harris, Blue Origin, and AFRL – Space Systems
Membership fees: $200,000
"BYU Site for SHREC I/UCRC"

Google
PI: Michael Wirthlin, 1/2021-12/2021, $40,000
"Automatic Detection of Sensitive Bits in FPGAs"

Google
PI: Brent Nelson, co-PI: Michael Wirthlin, 1/2020-12/2020, $40,000
"Open Source FPGA CAD Tools: Device Database Representations"

US Defense Thread Reduction Agency (DTRA)
PI: Michael Wirthlin, co-PI: Jeff Goeders, 1/2020-12/2024, $117,000 (additional pending)
"Cornerstone Workforce Development"

US Army
PI: Michael Wirthlin, 12/2019-10/2024, $225,000
"Cornerstone Workforce Development"

Cisco Systems
PI: Michael Wirthlin, 7/2020 – 6/2021, $40,000
"Detecting Silent Errors in FPGA-Based Networking Systems using Duplication with Compare (DWC)"

National Science Foundation SHREC Center: 2020
Sponsors: Sandia National Laboratories, BAE, Ball Aerospace, Raytheon, Lockheed Martin, L3Harris, AFRL – Sensors, and AFRL – Space Systems
Membership fees: $290,000
"BYU Site for SHREC I/UCRC"

Sandia National Laboratories: Dec 2019 – September 2021:
PI: Mike Wirthlin
"Fault-Injection and Scrubbing Infrastructure for Stratix X FPGA": $50,000

National Science Foundation SHREC Center: 2019
Sponsors: Los Alamos National Laboratory, Sandia National Laboratories, BAE, Ball Aerospace, Raytheon, Lockheed Martin, AFRL – Sensors, and AFRL – Space Systems
Membership fees: $330,000
NSF support (REU): $16,000
"BYU Site for SHREC I/UCRC"

National Science Foundation SHREC Center: 2018
Sponsors: Los Alamos National Laboratory, Boeing, Raytheon, NASA Goddard, Lockheed Martin, National Instruments, Boeing, Cisco, Altera, and AFRL – Space Systems
Membership fees: $290,000
NSF support (REU): $16,000
"BYU Site for SHREC I/UCRC"

National Science Foundation SHREC Center: 2017
NSF support ($150,000 x 3): $450,000
PI: Mike Wirthlin, Co-PI: Brent Nelson, Co-PI: Brent Nelson, Co-PI: Brent Nelson, 1/18-12/18
"BYU Site for SHREC I/UCRC"

Cisco Systems
PI: Michael Wirthlin, 10/2017 – 12/2018, $50,000
"Facilitating FPGA Fault Injection to Estimate SEU Sensitivity"

National Science Foundation CHREC Center: 2017
Sponsors: Los Alamos National Laboratory, Boeing, Raytheon, NASA Goddard, Lockheed Martin, National Instruments, Boeing, Cisco, Altera, and AFRL – Space Systems
Membership fees ($40k x 10): $400,000
NSF support (REU, Yearly Increment, and large site additional supplement): $96,000
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/17-12/17
"BYU Site for CHREC I/UCRC"

Cisco Systems
PI: Michael Wirthlin, 12/2016 – 10/2017, $35,000
"Evaluating the Effectiveness of pTMR with Embedded Fault Injection"

National Aeronautics and Space Administration (NASA): 2016
PI: David Long, Co-PI: Karl Warnick, Michael Wirthlin, and Brian Iverson, 5/16-5/18, $200,000
"Passive Inspection CubeSat (PIC)"

National Science Foundation CHREC Center: 2016
Sponsors: Los Alamos National Laboratory, Honeywell, Raytheon, NASA Goddard, Lockheed Martin, National Instruments, Boeing, Cisco, Altera, Xilinx, and AFRL – Space Systems
Membership fees ($40k x 11): $440,000
NSF support (REU, Yearly Increment, and large site additional supplement): $96,000
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/16-12/16
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2015
Sponsors: Los Alamos National Laboratory, Honeywell, Sandia National Laboratory, NASA Goddard, Lockheed Martin, National Instruments, and AFRL – Space Systems
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/15-12/15, $280,000
"BYU Site for CHREC I/UCRC"

Cisco Systems
Gift to support research in Partial TMR and FPGA Reliability, $80,000 (1/2014) "Self Recovery using Algorithmic Partial TMR (A-pTMR) "

National Science Foundation CHREC Center: 2014
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – APG, National Instruments, and AFRL – Space Systems
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/14-12/14, $240,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2013
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – SVIL, National Instruments, AFRL – Space Systems, Xilinx Corporation, and SEAKR Corporation
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/13-12/13, $320,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2012
Sponsors: Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, Lockheed Martin – SVIL, National Instruments, AFRL - Munitions, AFRL – Space Systems, Xilinx Corporation, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/12-12/12, $295,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center:2011
Sponsors: Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, Lockheed Martin – SVIL, National Instruments, AFRL - Munitions, AFRL – Space Systems, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/11-12/11, $295,000
"BYU Site for CHREC I/UCRC"

Cisco Systems
Gift to support research in Partial TMR and FPGA Reliability, $40,000 (08/2010)

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 09/10-5/11, $30,000
"Virtex 5 Self Scrubbing – Contract Extension"

National Science Foundation CHREC Center:2010
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, National Instruments, Rincon, NASA-Dryden, AFRL, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/10-12/10, $314,931
"BYU Site for CHREC I/UCRC"

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 10/09-9/10, $48,000
"Non-Volatile Memory Review and Analysis – Contract Extension"

National Science Foundation CHREC Center: 2009

Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, National Instruments, L3 Communications, Rincon, NASA-Dryden, SEAKR Corporation, and Xilinx Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/09-12/09, $420,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2008
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, NASA GFSC, Lockheed Martin, National Instruments, L3 Communications, Rincon
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/08-12/08, $278,275
"Brigham Young University To Join the I/UCRC CHREC Center"

Defense Advanced Research Project Agency (DARPA)
PI: Mike Wirthlin, Co-PI: Brent Nelson, Brad Hutchings, 9/07-7/08, $348,000
"Future FPGA Design Methodologies and Tool Flows"

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 9/07-8/08, $108,711
"Non-Volatile Memory Review and Analysis"

National Science Foundation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/07-12/07, $10,000
"Brigham Young University To Join the I/UCRC CHREC Center"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/07-12/09, $300,000
"Automated Design Techniques for Improving FPGA Fault Tolerance"

Lockheed Martin CE&T
PI: Michael Wirthlin, 9/06-9/07, $50,000
"Dynamic Internal Reconfigurable Technology"

Naval Undersea Warfare Center (NUWC)
PI: Steve Shultz, Richard Selfridge, and Michael Wirthlin, 5/06-10/08, $355,657
"Harsh Environment D-fiber Sensors (HEDS)"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/06-9/06, $50,000
"Reliability Modeling of the Xilinx VirtexII and Virtex4 FPGAs"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/04-12/06, $270,000
"Improving the Reliability of FPGA Designs through Automated Design Hardening"

Xilinx Corporation
PI: Brent Neslon, Co-PI: Michael Wirthlin, 4/04-4/05, $80,000
"Pro-Media Processor Development Kit"

National Aeronautics and Space Administration (NASA), sub-contract through USC-ISI
Sub-contract PI: Michael Wirthlin, 5/03-4/06, $150,000
"Reconfigurable Hardware IN Orbit (RHINO)"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/02-12/03, $120,000
"Improving the Reliability of FPGA Designs Operating in a Space Environment"

Defense Advanced Research Projects Agency
PI: B. Hutchings, Co-PI: B. Nelson, M. Wirthlin, and D. Wilde, 1999-2002, $2,489,870
"Unified Debug Environment for Adaptive Computing Systems"

Internally Funded Projects:

Ira Fulton College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2012-2013, $10,000
"Integrating FPGAs into Particle Physics Experiments"

Ira Fulton College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2005, $6,500
"Optimized Retiming and Operation Selection for Reconfigurable Data-Path Architectures"

Watson Embedded Systems Laboratory, Dept. of Electrical and Computer Engineering
M. Wirthlin, 2004-2005, $12,000
"High-Level Scheduling and Mapping Techniques for Reconfigurable Datapaths"
College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2000, $5,400
"Exploratory Research in Temporal Partitioning and Scheduling"

Graduate Students:

Dallin Skouson, Masters of Science, April 2022
"SpyDrNet – An Open Source Python Netlist Representation for Analysis and Transformation"
Andrew Keller, Doctor of Philosophy (PhD), December 2021
"Partial Circuit Replication for Masking and Detecting Soft Errors in SRAM-Based FPGAs"
Juan Andres Perez Celis, Doctor of Philosophy (PhD), December 2021
"Statistical Method for Extracting Radiation-Induced Multi-Cell Upsets and Anomalies in SRAM-Based FPGAs"
Corbin Thurlow, Masters of Science, June 2021
"TURTLE: A Fault Injection Platform for SRAM-Based FPGAs"
James Swift, Masters of Science, December 2020
"Root Cause Analysis and Classification of Single Point Failures in Designs Applying Triple Modular Redundancy in SRAM FPGAs"
Andrew Wilson, Masters of Science, June 2020
"Dynamic Reconfigurable Real-Time Video Processing Pipelines on SRAM-based FPGAs"
Brittany Wilson, Masters of Science, June 2020
"Evaluating and Improving the SEU Reliability of Artificial Neural Networks Implemented in SRAM-Based FPGAs with TMR"
Hayden Rowberry, Masters of Science, August 2019
"A Soft-Error Reliability Testing Platform for FPGA-Based Network Systems"
Matthew Cannon, Doctor of Philosophy (PhD), August 2019
"Improving the Single Event Effect Response of Triple Modular Redundancy on SRAM FPGAs Through Placement and Routing"
Jordan Anderson, Masters of Science, April 2019
"Neutron Beam Testing Methodology and Restuls for a Complex Programmable Multiprocessor SoC"
Luke Newmeyer, Masters of Science, April 2018
"Efficient FPGA SoC Processing Design for a Small UAV Radar"
Peter Zabriskie, Masters of Science, June 2018
"High Throughput FPGA Configuration Using a Custom DMA Configuration Controller"
Ammon Gruwell, Masters of Science, April 2017
"High-Speed Programmable FPGA Configuration Memory Access Using JTAG"
Andrew Keller, Masters of Science, April 2017
"Using On-Chip Error Detection to Estimate FPGA Design Sensitivity to Configuration Upsets"
Nathan Harward, April 2016
"Measuring Soft Error Sensitivity of FPGA Soft Processor Designs Using Fault Injection"
Aaron Stoddard, Masters of Science, December 2015
"Configuration Scrubbing Architectures for High-Reliability FPGA Systems"
Michael Gardiner, Masters of Science, July 2015
"An Evaluation of Soft Processors as a Reliable Computing Platform"
Josh Jensen, Masters of Science, April 2015
"Preemptive Placement and Routing for In-Field FPGA Repair"
Alex Harding, Masters of Science, June 2014
"Single Event Mitigation for Aurora Protocol Based MGT FPGA Designs in Space Environments"
Nathaniel H. Rollins, Doctor of Philosophy (PhD), April 2012
"Hardware and Software Fault-Tolerance of Softcore Processors Implemented in SRAM-Based FPGAs"
Patrick S. Ostler, Masters of Science, December 2011
"FPGA Bootstrapping Using Partial Reconfiguration"
Derrick S. Gibelyou, Masters of Science, August 2011
"Automated Fixed-Point Analysis and Bit Width Selection in Digital Signal Processing Circuits using Ptolemy"

Brian H. Pratt, Doctor of Philosophy (PhD), April 2011
"Analysis and Mitigation of SEU-induced Noise in FPGA-based DSP Systems"
William A. Howes, Masters of Science, April 2011
"On-Orbit FPGA SEU Mitigation and Measurement Experiments on the Cibola Flight Experiment Satellite"
Adam Arnesen, Masters of Science, April 2011
"Increasing Design Productivity for FPGAs through IP Reuse and Meta-Data Encapsulation"
Jonathon Johnson, Masters of Science, April 2010
"Synchronization Voter Insertion Algorithms for FPGA Designs Using Triple Modular Redundancy"
Welson Sun, Doctor of Philosophy (PhD), April 2008
"Using duplication with compare for on-line error detection in FPGA-based designs"
Dan L. McMurtrey, Masters of Science, December 2006
"Using duplication with compare for on-line error detection in FPGA-based designs"
Keith S. Morgan, Masters of Science, August 2006
"SEU-Induced Persistent Error Propagation in FPGAs"
D. Eric Johnson, Masters of Science, August 2005
"Estimating the Dynamic Sensitive Cross Section of FPGA Design Through Fault Injection"
Matthew R. Koecher, Masters of Science, December 2003
"Hardware Synthesis of Synchronous Data Flow Models"
Brian J. McMurtrey, Masters of Science, April 2003
"Approaches in Web Based Design and Evaluation of Digital Circuits"
Benjamin L. Bullough, Masters of Science, August 2002
"Analysis of Field-Programmable Gate Array Implementations of Constant Coefficient Finite Impulse Response Filters"
Wesley J. Landaker, Masters of Science, August 2002
"Using Hardware Context-Switching to Enable a Multitasking Reconfigurable Computer System"
Steven E. Morrison, Masters of Science, April 2001
"Design and Performance Analysis of a Configurable Hardware Solution of an Adaptive Automatic Target Recognition Algorithm"